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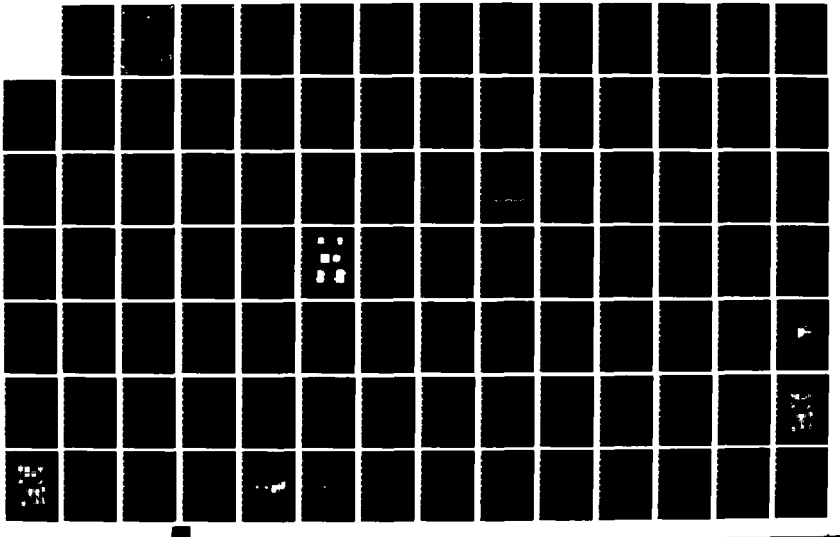

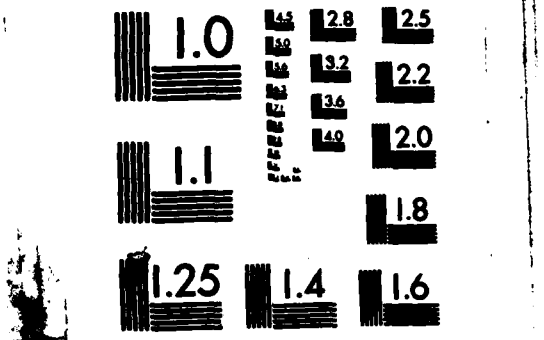

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THE DESIGN AND LAYOUT OF A COMPLEMENTARY METAL OXIDE SEMICONDUCTOR SILICON ON SAPPHIRE CELL LIBRARY

THESIS

AFIT/GE/EE/83D-62 Wayne E. Sommars
Captain USAF

DEPARTMENT OF THE AIR FORCE
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THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by
Wayne E. Sommars, B.S.
Captain USAF
Graduate Electrical Engineering
December 1983

Preface

Throughout this project, a method for developing CMOS/SOS designs has been documented. My intent has been to compile an information base from which future AFIT design efforts may draw in order to avoid the difficulties I experienced. In doing so, a small CMOS/SOS cell library, a 4-bit ALU, and a PLA generator were developed. Though none have been validated, I challenge potential thesis students to continue this project with the intent of developing a test method for verifying CMOS/SOS designs.

Since early undergraduate studies, I have had a strong interest in solid state physics and semiconductor design. My AFIT tour has given me the opportunity to further my education in these fields and in particular, to concentrate in computer-aided IC design. Selection of this thesis topic as the culmination of my curriculum proved to be a tremendous and successful learning experience.

I offer a special thanks to Hal Carter, my thesis advisor, for allowing me to take on this thesis project and for his overall assistance and draft reviews. My appreciation also goes to Roger Colvin for helping me to understand SPICE models, providing draft reviews, and for his technical guidance. I am also indebted to Chuck Seitz of Caltech whose unpublished text provided much of the background for my thesis research.

Wayne Sommars

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Abstract

A method was developed for designing CMOS/SOS circuits using computer-aided design tools available from Stanford University and The University of California at Berkeley. CMOS/SOS fabrication methods and theory of operation as well as differences between CMOS/SOS and bulk CMOS were researched. SPICE was used to determine optimum gate width-to-length ratios resulting in symmetrical transitional delays.

Two designs were developed to implement the CMOS/SOS programmable logic array (PLA), and a "C" program was written to automatically generate one of the designs by means of a file formatted in Caltech Intermediate Form (CIF). Basic logic gates were designed as part of a small CMOS/SOS standard cell library, and a medium scale integration (MSI) arithmetic logic unit (ALU) was developed using cells from the library.

An analysis was made of significant differences between a NMOS PLA developed by Stanford and the CMOS/SOS PLA. According to SPICE results, the CMOS/SOS PLA exhibited slightly faster switching speeds and greatly reduced power dissipation. CMOS/SOS circuits required significantly larger layouts than similar NMOS circuits.

THE DESIGN AND LAYOUT OF A COMPLEMENTARY METAL OXIDE SEMICONDUCTOR/SILICON ON SAPPHIRE CELL LIBRARY

I. Introduction

Background [Ref 1:1-4]

During the mid-1970s, the Department of Defense (DOD) and the National Aeronautics and Space Administration (NASA) recognized the universal requirement for enhanced microelectronics for current and future space and weapons systems. Space systems exposed to various levels of radiation were experiencing performance degradation, data loss, and other forms of logic upset including latch-up.

All of the popular semiconductor technologies at the time were susceptible to these problems, and none satisfied the additional requirements of low power consumption, high density, and high switching speeds critical to space systems or portable weapon systems. Bulk Complementary Metal Oxide Semiconductor (CMOS) electronics were effective in reducing radiation effects and required minimal power; however, these devices suffered from slow switching speeds and could not be expected to provide the high throughput signal and data processing needs of the mid-1980s and beyond. Given these limitations and requirements, the Air Force Avionics and Materials Laboratories began exploratory development into various promising semiconductor technologies. CMOS circuits built on sapphire substrates, CMOS/SOS, has emerged as the only technology to simultaneously meet these requirements.

CMOS/SOS exhibits all of the desirable characteristics of the standard bulk CMOS process such as low power consumption, excellent noise immunity, and wide operating-temperature range. It is also faster, has better radiation resistance, and is easier to fabricate. Additionally, CMOS/SOS is comparable to Transistor-Transistor Logic (TTL) in switching speed and is second only to N-Metal Oxide Semiconductors (NMOS) in circuit density. Because of these characteristics, the DOD has awarded numerous contracts for the development of CMOS/SOS circuits as part of the DOD sponsored Very High Speed Integrated Circuit (VHSIC) program.

One of the major objectives of this $325 million program is the development of high throughput signal and data processing capabilities for military systems such as the NAVSTAR Global Positioning System and other space and satellite systems [Ref 2:I-27]. In line with this objective are the additional objectives of enhanced radiation tolerance, low power, and high density demanded by the space environment. Currently, several manufacturers and universities are conducting DOD sponsored research and development efforts with CMOS/SOS semiconductors to meet these needs.

Because of the increasing popularity of CMOS/SOS as a VHSIC technology, military engineers must become knowledgeable in CMOS/SOS characteristics and skilled in its design and layout if they are to effectively manage VHSIC

programs. Currently however, military engineering students at the Air Force Institute of Technology (AFIT) are able to design and layout only NMOS circuits. Several computer-aided design (CAD) tools are available for this purpose, such as the Stanford University Chip Layout Language (CLL), a program for checking geometrical design rules, and an event-driven switch-level simulator [Ref 3]. Also available is the Stanford NMOS cell library which consists of modular circuits designed and layed out using these tools [Ref 4].

CMOS/SOS however, is a relatively new technology which has few established design procedures and virtually nonexistent computer aided design tools, at least at the university level. As a result of the intense DOD interest in CMOS/SOS technology, this thesis project will be conducted to provide the core material required for future engineering students at AFIT to be able to confidently design and layout CMOS/SOS circuits. This thesis should also establish the ground work necessary for future thesis research in this area.

Problem Statement/Scope

The purpose of this thesis will be to provide a comprehensive analysis of CMOS/SOS semiconductors, from principles of operation to circuit design, fabrication, and layout, and also to design a working CMOS/SOS cell library using modified and unmodified CAD tools available at AFIT.

No attempt will be made to design a completely new set of CAD tools applicable only to CMOS/SOS. Rather, where appropriate, existing tools will be modified to better facilitate CMOS/SOS design procedures.

As noted earlier, the Stanford CLL is used extensively in NMOS design by AFIT graduate students. The students use CLL to specify the locations of semiconductor components and connections on an integrated circuit. CLL then produces a data file, formatted in Caltech Intermediate Form (CIF), which may be sent to a manufacturer for fabrication into a working integrated circuit. Currently, however, CLL only supports the design of NMOS semiconductors. In order to design CMOS/SOS circuits, it is necessary to modify the CIF files produced by CLL in order to arrive at a format acceptable for fabrication. An alternative method is to modify CLL to provide the correct CIF file so that student effort is minimized. This thesis will describe the former approach.

Another CAD tool that is frequently used at AFIT is the Stanford programmable logic array (PLA) generating program, PLAGEN [Ref 3]. Given a truth-table-like input of the desired functions, this program produces a CIF file ready for fabrication. Thus, the time consuming process of designing and laying out a PLA by hand is eliminated. This particular program uses predefined pieces of the PLA planes (layers comprising the PLA AND/OR circuitry), designed as CIF library cells, to generate the appropriate PLA CIF file.

The PLA normally consists of two distinct sections called AND and OR planes, which generate product and sum-of-product terms respectively. A complete CMOS/SOS library of the required PLA cells will be designed, and PLAGEN will be modified to produce the required CIF file.

The design and layout of any semiconductor circuit is always easier if the designer has access to a library of standard cells which have been designed and tested. This relieves the designer from the time consuming task of redesigning and debugging the most basic components common to most systems. The ideal cell library consists of circuits that can easily be used as building blocks to develop medium and large scale integration designs. It is also important that these library cells have geometrically minimum areas and adhere to all geometrical design rules. A small CMOS/SOS cell library will be designed and layed out, and a 4-bit Arithmetic Logic Unit (ALU) will be designed and layed out using these same library cells. Due to the amount of time alloted to complete this thesis, no attempt will be made to physically test the ALU or individual components of the cell library, nor will an attempt be made to design a cell library as extensive as the Stanford NMOS cell library. Hopefully, these tasks will be accomplished by later thesis work or by students of future semiconductor design classes at AFIT.

To provide the background necessary to properly design and layout CMOS/SOS circuits, one chapter of this

thesis will be dedicated as a tutorial to future engineering students at AFIT. The information to be provided will, hopefully, be sufficiently detailed to be used as class notes.

Assumptions

The following assumptions were made to narrow the thesis problem to one which could be handled during the alloted time:

1. Tested and working input, output, VDD, and ground pads are assumed to be available as library functions or as CIF files. The design and testing of pads is a sufficiently complex task to warrant an entire thesis effort by itself. Many considerations, such as pad transistor breakdown voltages and appropriate protection devices, must be considered.

2. A program to check CMOS/SOS design rules should become available from other university work before this thesis is completed. If not, then the Stanford NMOS design rule checking program may prove useful in detecting basic CMOS/SOS design rule errors. Certain design rules, such as metal, poly, and diffusion minimum width criteria as well as metal-to-metal separation are the same for both technologies.

3. Throughout this thesis, a basic understanding of semiconductor technology and design, as well as a thorough knowledge of existing CAD tools at AFIT, is assumed on the part of the reader.

Summary of Current Research

The majority of research being conducted in the CMOS/SOS area is a direct result of the VHSIC program. As previously mentioned, several manufacturers are involved in

the production of CMOS/SOS devices to meet DOD signal and data processing needs. And, as expected, a tremendous amount of state-of-the-art information has been compiled regarding this technology. However, VHSIC is controlled under the International Traffic in Arms Regulation (ITAR), and as such, most VHSIC literature is releasable only to DOD agencies and approved contractors [Ref 5:I5-I7]. Therefore, the information presented in this section and throughout the rest of this thesis is information gathered from non-controlled sources.

Of the manufacturers known to be involved in VHSIC CMOS/SOS related developments, RCA and TRACOR INC. have jointly developed a high performance, expandable, microcomputer chip set. The heart of the chip set is an 8-bit slice processing unit, designated GPU for general processing unit, that has been used in GPS ground receivers and to emulate the PDP-11 and AN-UYK-20 Standard Navy Computer [Ref 6]. The chip set may be customized to other unique military applications using RCA CMOS/SOS universal gate arrays. Additionally, Hughes Aircraft Co. in conjunction with Perkin Elmer/ETEC has developed a CMOS/SOS digital correlator and algebraic encoder/decoder spread spectrum subsystem to be used in the Battlefield Information Distribution Subsystem (BIDS) [Ref 7:84,85].

Several universities are independently experimenting with classes in bulk CMOS design; however, the California Institute of Technology (Caltech) is the only university

known to have a CMOS/SOS design course. Though no text is currently available, much of the instructional material for the course was taken from notes written by Chuck Seitz, also of Caltech. His notes will also provide the raw material required for the formulation of this thesis [Ref 8]. A large portion of university related research into CMOS/SOS design has been sponsored by the Defense Advanced Research Projects Agency (DARPA).

Approach

The approach used in this thesis will be to first compile a working knowledge of the CMOS/SOS process, to include principles of operation, electrical characteristics, geometrical design rules, and general design procedures. The existing CAD tools used at AFIT will then be analyzed to determine the procedures and modifications required to facilitate CMOS/SOS design. The extent of the modifications will be based upon a careful analysis of student interface requirements, ease of implementation, and functional tradeoffs. Once determined, the appropriate changes will be made to PLAGEN. Additionally, the process of manually modifying the CIF file produced by CLL will be documented.

Once this part of the thesis is completed, the specification of the cell library and PLA pieces library will be formulated. The library cells will then be designed and layed out. Following standard cell library completion, the ALU will be layed out so as to best utilize the

interface features of the different cells. Lastly, the modified version of the PLA generator will be demonstrated, and all library cells will be simulated.

Sequence of Presentation

Chapter II is a tutorial presentation of CMOS/SOS principles, fabrication, and design. Similarities and significant differences between CMOS/SOS and bulk CMOS are also discussed. Those readers familiar with CMOS/SOS technology may skip chapter II without loss of continuity.

Chapter III presents the characteristics and requirements, along with appropriate justification, of individual cells and the cell library. Included are the requirements and characteristics of basic logic gate cells, a bit slice ALU, and a CAD tool which will generate the CMOS/SOS PLA. Documentation and interface requirements are also discussed.

Chapter IV provides the system level designs of the ALU and PLA generator. A block diagram of the ALU, based on the full adder circuit, is presented. Also included is a circuit-level diagram of a example CMOS PLA to show the reader its basic composition. Additionally, a structure chart of the CMOS/SOS PLA generator is briefly discussed.

Chapter V establishes the detailed designs of all standard cells, the ALU, and the software for the PLA generator. SPICE simulations for most standard cells as well as the PLA are introduced to verify designs. Standard

cells are presented as CLL layouts, and their operation and special features are discussed. The standard cells are used to implement the ALU, which is diagramed at its logic gate level. Additionally, two methods of implementing the layout of the CMOS/SOS PLA are presented. The software design of the PLA generator is discussed, and appropriate structure charts are provided.

Chapter VI analyzes the CMOS/SOS PLA and PLA generator performance as compared to the Stanford NMOS PLA and PLA generator PLAGEN. The CMOS/SOS ALU is compared to a NMOS PLA previously designed by this author. The standard cell library is also compared to the Stanford NMOS cell library.

Chapter VII presents this authors conclusions and recommendations for future CMOS/SOS design at AFIT.

II. CMOS/SOS Devices and Circuits

CMOS/SOS is a relatively new technology in which CMOS circuits are built on sapphire substrates rather than bulk silicon, as in the standard CMOS process. The major affect of this structural difference is a reduction in parasitic capacitances, which results in enhanced electrical characteristics. This chapter presents a comprehensive analysis of CMOS/SOS characteristics as well as CMOS/SOS device fabrication. Similarities, as well as significant differences, between bulk CMOS and CMOS/SOS are also presented. This chapter is intended as a tutorial which should enable the reader to attempt the design of CMOS/SOS circuits with reasonable confidence.

The CMOS Circuit

All CMOS semiconductors provide both n channel(NMOS) and p channel(PMOS) transistors on the same substrate. Those readers familiar with NMOS technology will recall that enhancement mode NMOS transistors have no conducting channel at zero gate-source voltage and, as a result, are normally off. Current begins to flow through this type of device only when the gate-source voltage is greater than the device threshold voltage, typically 0.2Vdd [Ref 9:3]. The depletion mode NMOS transistor has a conducting channel at zero gate-source voltage and is normally on.

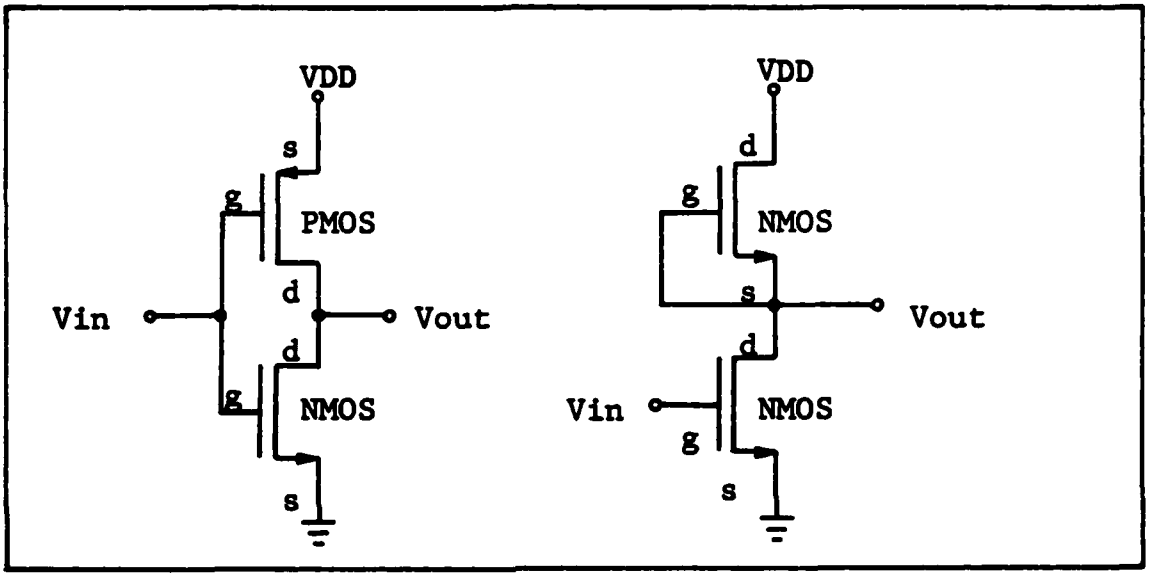
The PMOS transistor is similar to the NMOS

transistor but operates with bias voltages of opposite polarities. Hence, assuming TTL compatible voltages, the enhancement PMOS is normally off at a bias of 0 volts but begins to conduct current as the gate-source voltage becomes negative with respect to the device threshold voltage, usually -0.2Vdd. Analogously, the depletion mode PMOS is normally on at a gate-source bias voltage greater than the threshold voltage. The channel for this type of device becomes depleted as the gate-source voltage becomes more negative than the threshold voltage.

While both enhancement and depletion devices are normally used in individual NMOS or PMOS circuits, depletion mode devices are rarely used in CMOS designs [Ref 10:43]. This results from the symmetrical but opposite switching voltages of NMOS and PMOS enhancement transistors. Thus, instead of using passive pull-up and active pull-down transistors, CMOS circuits use both active pull-up and active pull-down gates (when in the active state, pull-up transistors provide a conducting path to Vdd, and pull-down transistors provide a path to ground).

The main advantage of this unique arrangement is that power is drawn only during transient conditions, when gate-source voltages change state. In fact, CMOS is the only technology in which power is consumed only during logic transitions. In the static data condition, minimal power is drawn in the form of junction leakage currents [Ref 11:150]. An examination of the most basic CMOS circuit, the CMOS

inverter of Figure II-1a, illustrates the arrangement of NMOS and PMOS gates necessary to achieve complementary switching. (throughout this paper, NMOS and PMOS gates will be identified as follows: NMOS gates will be represented by an arrow pointing from gate to source, and PMOS gates will be represented by an arrow pointing from source to gate).



(a) (b)

CMOS Inverter NMOS Inverter

Figure II-1

Note that the two transistors share a common gate and common drain and that the source voltages are at opposite polarities. When a logic 0 is applied to the CMOS inverter input, the lower NMOS gate-source voltage = 0V, and the gate is switched off. However, the gate-source voltage of the upper PMOS gate = -Vdd , which causes the gate to switch on, and ties the output high. Conversely, a logical 1 applied to the inverter input causes the p channel gate to

switch off while the n channel gate switches on, resulting in the output being tied to ground.

In the steady-state condition, regardless of the input voltage, one of the CMOS gates is switched off. As a result, no conducting path from Vdd to ground is available, and the CMOS gate draws no power except for power dissipated through junction leakage. This very small leakage current is due to the reverse bias leakage current of the p-n junction of the off transistor. Ordinary room temperature leakage currents of reverse biased p-n junctions are in the nanoamp to picoamp range, with resultant power dissipation in the nanowatt to picowatt range [Ref 12:178]. In comparison, the NMOS inverter of Figure II-1b draws minor leakage current only when the input is low and the output is high. When the input is high, the output is switched low, and the gate constantly draws whatever power it was designed for. Of course, this power consumption is directly related to the length-to-width ratio of the NMOS depletion mode pull-up transistor. Power dissipation is typically in the milliwatt to microwatt range.

DC Analysis

Typical I-V characteristics of MOS n channel and p channel devices are illustrated in Figures II-2a and b. Figure II-2a clearly shows that the PMOS enhancement device conducts current only when the drain-source bias is more negative than some arbitrary threshold voltage. This

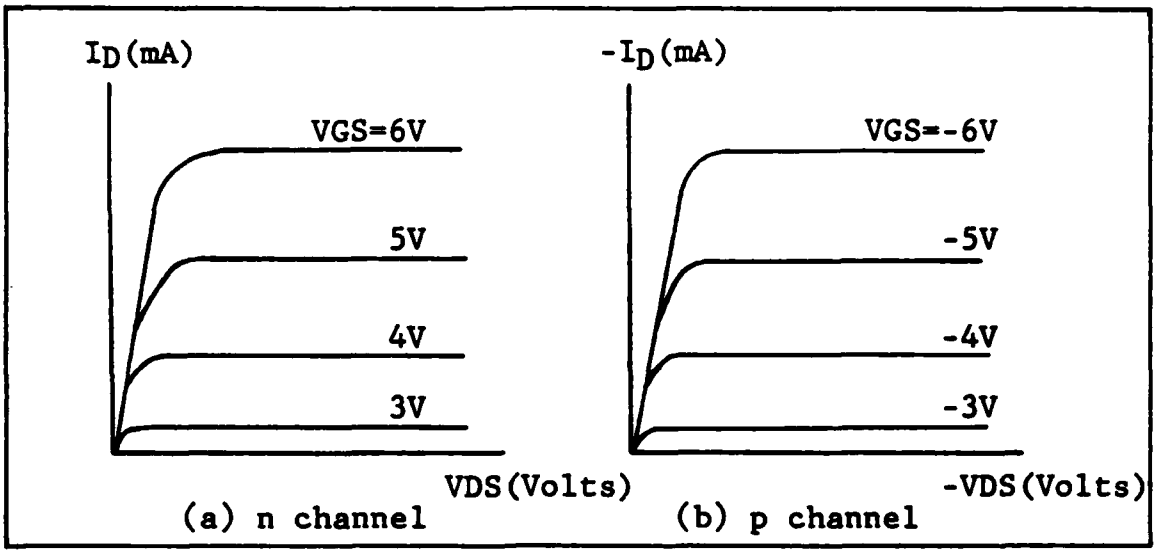


Figure II-2 [Ref 13:C.2A.20-21]

voltage is set by the manufacturer during the fabrication process, and for CMOS devices corresponds to about -1V for TTL compatible devices.

Since complementary switching is desired for both p channel and n channel devices, in the steady state, the Ids (drain-to-source current) for both transistors is

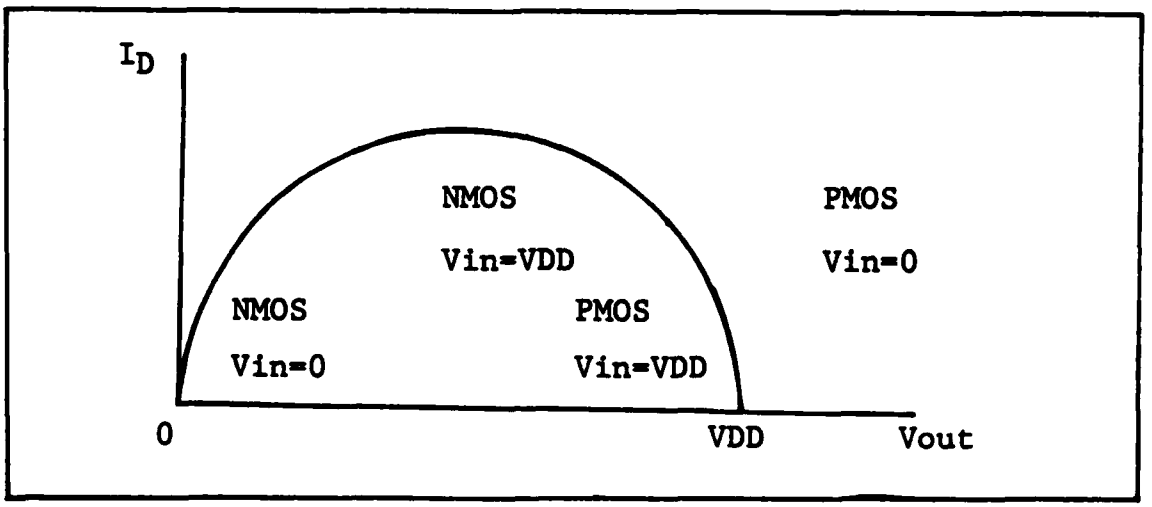


Figure II-3 CMOS Load Line [Ref 10:98]

ideally symmetrical but opposite. A graphical representation of the CMOS load line may be obtained by first graphically superimposing the two plots shown in Figure II-2. The load line of Figure II-3 is derived from Figure II-2 by noting that since the voltage characteristics of both devices must be symmetrical, only one of the PMOS curves is considered, namely the one for a saturated drain-source voltage of -5V.

The significance of Figure II-3 is that the drain-source current peaks at a Vds between high and low logic level input voltages. As the Vds voltage approaches 0 or Vdd, the drain-to-source current theoretically approaches zero. Thus, the minimal power requirements of CMOS circuits mentioned earlier are justified. The intersection of the PMOS load line with the characteristic curves of the NMOS gate results in the CMOS voltage transfer characteristic of Figure II-4. This procedure is analogous to intersecting the depletion load line of the NMOS inverter with its characteristic curves to arrive at the NMOS transfer characteristic (see Mead and Conway pp.7-8) [Ref 9].

If NMOS and PMOS gates had identical properties, complete symmetry would exist between Vout and Vin. However, since the gate of a NMOS device is normally positive with respect to the substrate, positively charged ions collect along the SiO_2 substrate interface and reenforce the action of the positive gate bias. The result is a slightly asymmetrical voltage swing because the NMOS

device tends to turn on prematurely. With PMOS devices, positive ions are pulled to the opposite side of the oxide layer formed by the gate-oxide interface and do not effect device switching [Ref 14:326,327].

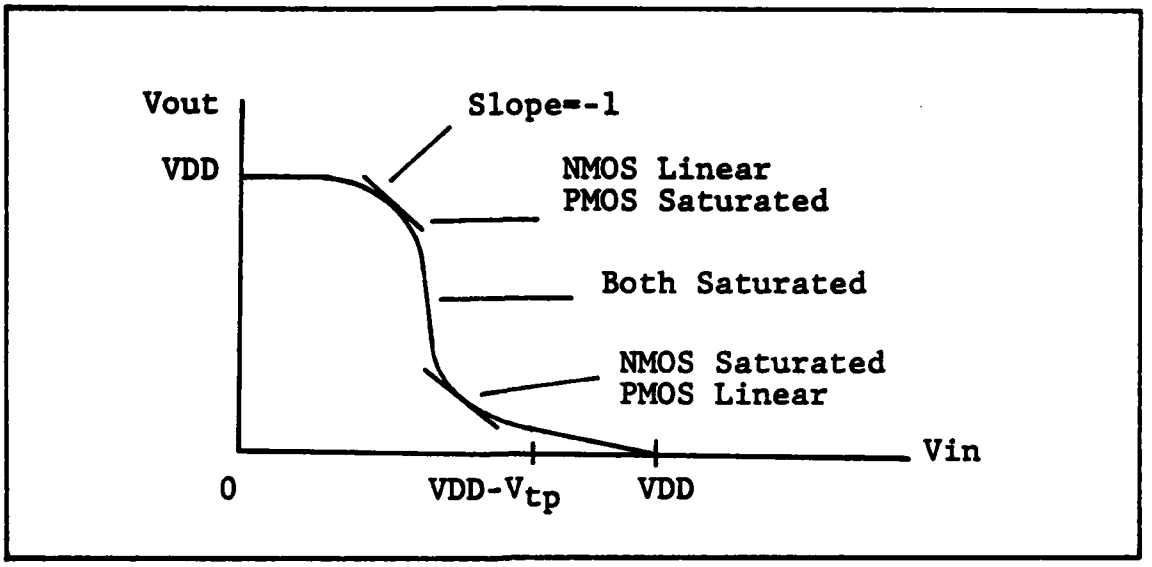


Fig. II-4 CMOS Voltage Transfer Characteristic [Ref 10:98]

Circuit Delay [Ref 8]

CMOS has been described as a "ratioless" technology, indicating equal width-to-length ratios for pull-up and pull-down transistor networks. This is thought to be acceptable because delay responses have been shown to be relatively broadbanded for ratios varying from 1:1 to 3:1 and centered around a minimum for a ratio of 1.4:1. This section provides an analysis of CMOS width-to-length ratios and corresponding delay times, and provides a basis for selecting a standard ratio to be used throughout the design portion of this thesis.

The task of determining CMOS circuit delay is not as

simple as that for NMOS since n and p channel devices have inherently different mobilities and thus, different propagation delays. This is due to the fact that NMOS semiconductor devices rely on electrons as minority carriers whereas PMOS devices rely on holes as minority carriers. Though the mobility of both electrons and holes is a function of impurity concentration and temperature, Seitz' measured values indicate that electron mobility is generally twice that of hole mobility for CMOS/SOS. Data from the proposed manufacturer of CMOS/SOS devices for AFIT corroborates these values. Thus, the gate delay for p channel devices is approximately twice the gate delay of n channel devices for the same areas. Hence, any asymmetrical high-going or low-going gate delay in CMOS circuits is a result of the differences in electron and hole mobilities. In contrast, asymmetrical gate delay for purely n channel or purely p channel devices is strictly a function of gate geometries (gate delay increases as length-to-width ratios are increased to provide larger fanout as well as larger gate capacitive driving capability). This is due to the passive pull-up gate being able to supply only a fraction of the current supplied by the pull-down gate.

It seems logical that to achieve symmetrical rise and fall times for CMOS n channel and p channel gates, the overall transconductances of each gate must be made similar. Recall that transconductance is a product of the gate oxide capacitance and device mobility. Thus, the obvious

conclusion is to assume symmetry can be achieved by specifying a 2:1 width-to-length ratio of p to n channel gates, which would compensate for the difference in mobilities between NMOS and PMOS devices. Hence, the p channel gate would be twice as wide as the minimum width n channel gate.

Although this practice is often used in industry, evidence suggests within certain geometrical tolerances the ratio of p to n channel gates does not significantly affect gate delay. One reason is that the minority carriers of p channel gates (holes) are less efficient at converting gate charge to source-to-drain current. Thus, as the width of the p channel gate is increased, the delay time increases only slightly for large increases in geometry. And as the the p channel gate delay decreases, the possibility exists that the n channel gate, if already employing minimum geometry, will become the limiting delay factor. Seitz's calculated theoretical propagation delays for various ratios indicate that delays are identical for both 1:1 and 2:1 p channel to n channel ratios. He bases this result on a "Tau" delay estimation model which is based on the observation that minimum length transistors drive current in proportion to their own gate capacitance. The Tau model also indicates a minimum delay response for 1.4:1 ratios.

This author ran several SPICE simulations of a typical CMOS/SOS inverter to attempt to verify the accuracy of the Tau model. The ratios of the simulated pull-up to

pull-down transistors were 1:1, 1.4:1, 2:1, and 3:1. Four micron geometry was assumed, and hole surface mobilities of 200 cm2/V-sec and electron surface mobilities of 400 cm2/V-sec were used. Other parameters were taken directly from specifications supplied by the manufacturer for CMOS/SOS circuits. The specifications, along with original SPICE results, are listed in Appendix A. These same specifications will apply to CMOS/SOS circuits manufactured for future AFIT VLSI design classes.

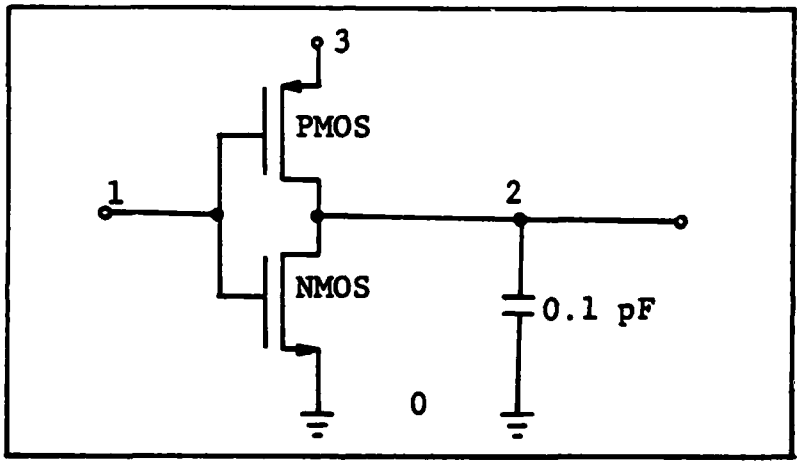


Figure II-5 SPICE CMOS/SOS Inverter Model

In all simulations, the input is a 5V pulse with a 1.0 nsec delay, zero rise and fall times, and a duration of 10 nsec. The initial input was 0v, and all responses are plotted from 0 nsec to 20 nsec. This particular gate input was used because it resulted in an optimum comparison of both rise and fall delay times. The MOSFET model used in this simulation, with appropriately labled SPICE nodes, is shown in Figure II-5.

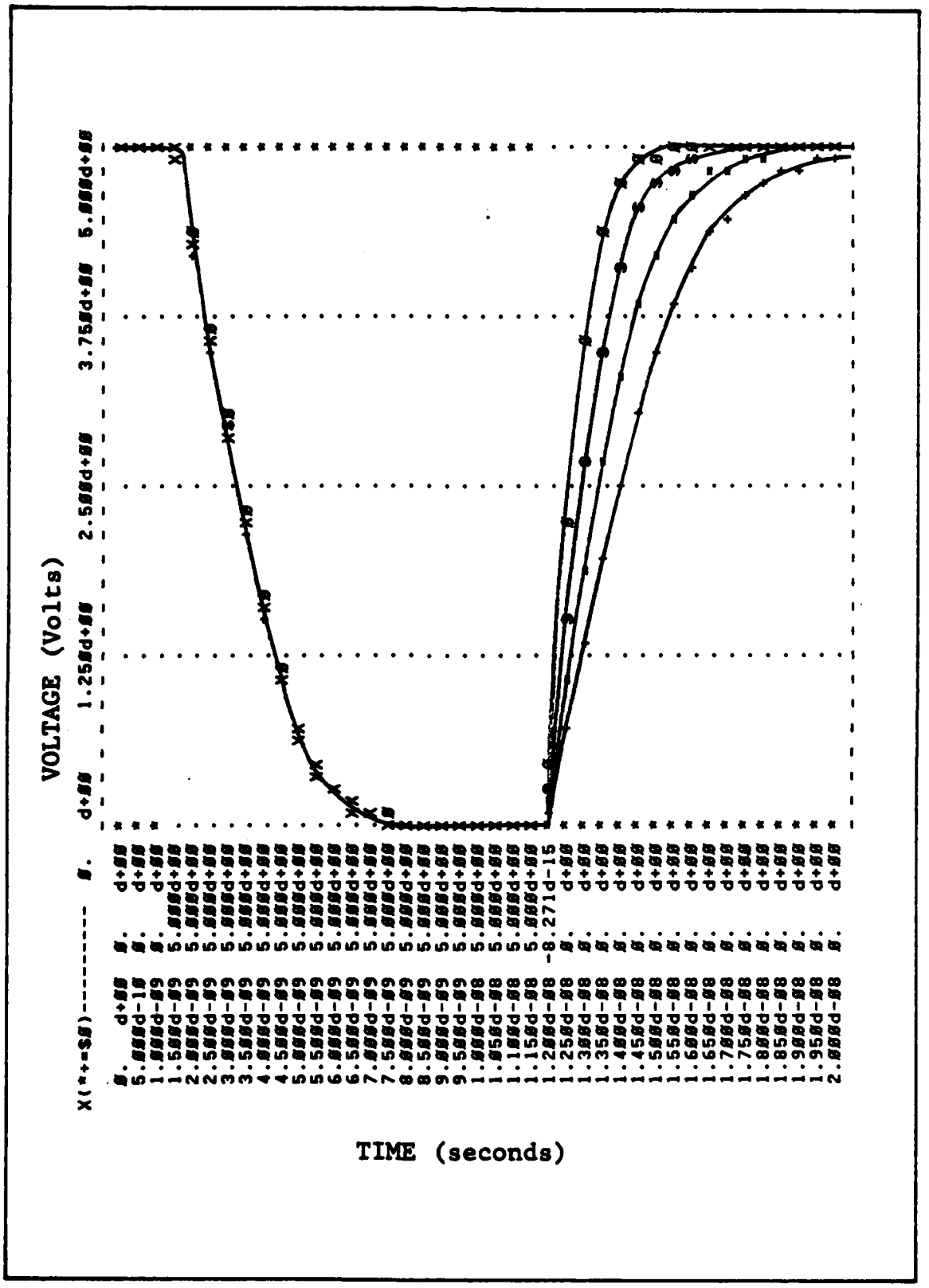


Figure II-6 Inverter Transient Responses

Figure II-6 shows the transient time responses for 1:1, 1.4:1, 2:1, and 3:1 width-to-length ratio CMOS/SOS inverters. The ratios are plotted as follows: Input = '*', 1:1 = '+', 1.4:1 = "=", 2:1 = '$', 3:1 = '0'. According to these simulation results, the most symmetrical rise and fall responses do, in fact, occur for 1.4:1 ratios. However, 1:1 ratios clearly result in noticeably longer rise times. Additionally, the curve representing the width/length ratio of 3:1 (plotted as 0's) corroborates Seitz other claim that a ratio that is too large will result in the NMOS device becoming the limiting factor in circuit performance. Since the NMOS gate is already at 4 micron geometry, the standard 1982 geometry, nothing is gained by making the PMOS ratio greater than 1.4:1, other than ease of design.

Evidence suggests that this analysis will not require revision as geometries scale to micron or submicron levels. The fundamental properties affecting the rise and fall delays of both transistor types are electron and hole mobilities, which remain unaffected by geometry. The one affect that will occur though, will be a significant reduction in overall gate delay. Since gate capacitance is determined by the permitivity of the oxide times the gate area divided by the separation of the gate oxide, overall gate capacitance will decrease. As a result, the time required to charge the gate capacitance (and other parasitics) will be reduced.

Certain limitations inherent in both simulation

models must be recognized before a standard practice is decided upon. That is, the models are only as accurate as their input parameters. Though the input parameters for the SPICE simulation are believed to be accurate, they undoubtedly do not precisely model a CMOS/SOS inverter. Possibly, the only true verification method is the actual testing of physical devices. Nevertheless, the SPICE program has been used since 1976 and has become an almost universal simulation model for MOSFETS and other types of transistors. Though the 1.4:1 ratio provides the most symmetrical delay, the industry standard has been to use 2:1 ratios of PMOS to NMOS gates. For this reason, and to simplify design and layout procedures, all inverters and transistor pair designs in this thesis will use 2:1 ratios.

Before the reader assumes that 2:1 ratios are acceptable for all CMOS/SOS designs, a few words of caution are in order. Unlike the basic inverter, several circuits, such as the NAND and NOR gate, do not use transistors in pairs. Rather, in these circuits, several transistors are connected in series and in parallel, which tends to negate the symmetry arising from 2:1 ratios. Thus, calculations or SPICE analyses are necessary to arrive at optimum ratios for each different circuit. This anomaly will be discussed in greater detail in Chapter V.

Other possible exceptions may arise where inverters are used to drive large capacitive loads. The usual CMOS practice for this instance is to make use of precharge

networks, which maintain inputs at a high logic level. This reduces the delay time normally associated with pull-up networks since a line can normally be discharged faster than it can be charged. Another practice is the use of double buffered outputs which consist of two stages of inverters, each with successively wider gates for both the PMOS and NMOS devices.

CMOS and CMOS/SOS Fabrication [Refs 6,8,15:51]

CMOS circuits can be fabricated using either bulk silicon or sapphire substrates. The bulk silicon process is similar to the NMOS process except for additional steps required to form silicon dioxide (SiO_2) isolation wells and a "p" type well for the "n" channel (NMOS) transistor. Figure II-7 illustrates this process which begins with an epitaxially grown "n" type substrate.

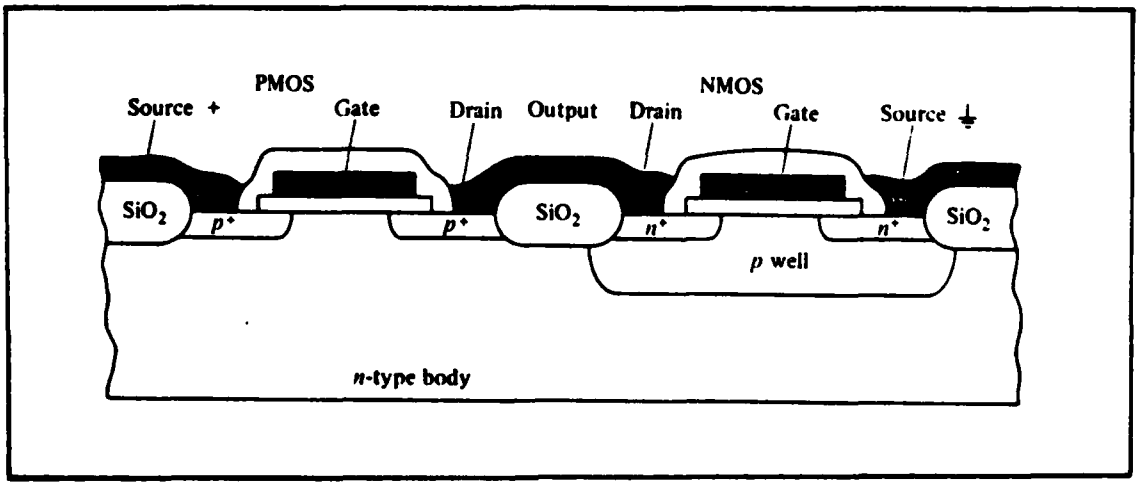


Figure II-7 Bulk CMOS Cross-Sectional View [Ref 10:42]

The first mask defines a region which is exposed to a "p" type impurity such as Boron. This step defines the "p" type well required by the NMOS transistor. Another mask defines the source and drain of the PMOS transistor which receives a heavier doping of Boron, leaving these areas doped "p+". The next step requires a definition of the source and drain of the NMOS transistor. This area of the wafer is exposed to a "n" type doping material such as Phosphorus, Arsenic, or Antimony, resulting in a "n+" doped source and drain.

A process step that is usually included is the definition of isolation wells, formed by etching the silicon substrate and growing SiO_2 in the etched areas. This step aids in the reduction of parasitic transistors formed between adjacent "n" channel (NMOS) and "p" channel (PMOS) transistors. Parasitic transistors are a major cause of bulk CMOS latch-up. The problem of latch-up does not occur in CMOS/SOS for reasons that are discussed in a later section.

The remaining steps are similar to the NMOS process in which gate oxide is formed, silicon gates are grown, metal connections are formed, and the chip is coated with an overglassing of SiO_2 for protection. Due to the requirement for isolation areas, the bulk silicon process does not exhibit the circuit densities found in NMOS designs. While, as mentioned previously, isolation wells reduce the effects

of parasitic transistors, gate-substrate capacitance and other capacitances are not reduced by isolation wells. Gate-substrate capacitance is common to both bulk and CMOS/SOS processes, but other capacitances are found to a much greater extent in bulk CMOS.

The CMOS/SOS process is significantly different from bulk CMOS and results in an almost total elimination of parasitic transistors and resultant latch-up. This is because the CMOS/SOS process begins with a sapphire substrate on which an epitaxial layer of silicon is grown.

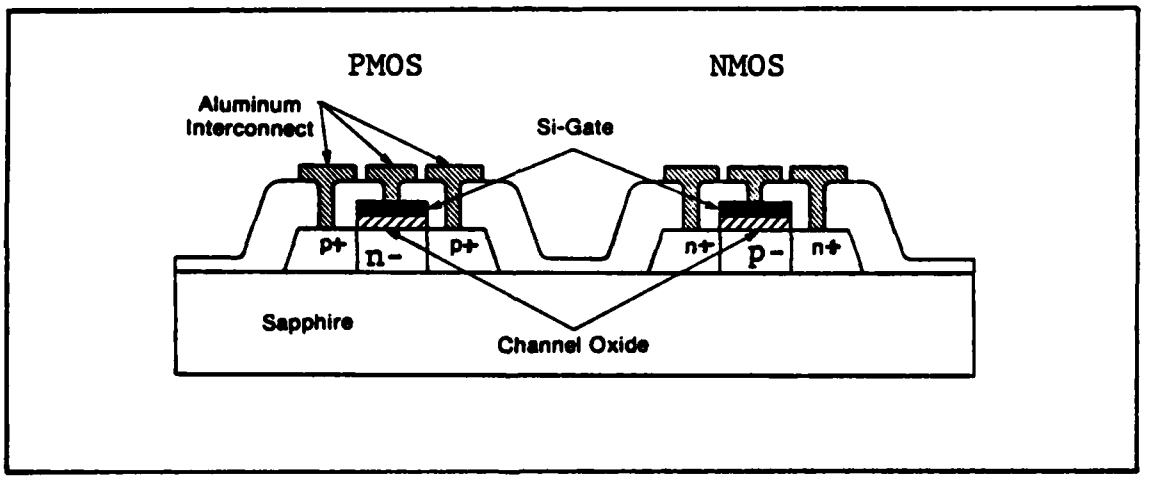


Figure II-8 CMOS/SOS Cross-Sectional View [Ref 6]

The second process step is the definition and masking of all areas where transistors are to be formed. The epitaxial layer is then etched to the bare sapphire, leaving island areas composed of silicon. With the alternative isoplanar process, a thin layer of epitaxial silicon is left, and SiO_2 is grown between the islands to make the surface flatter. Though the conventional process

is illustrated in Figure II-8, both processes result in functionally identical devices.

The next step in the CMOS/SOS process is the definition of "n" type (NMOS) islands by means of an implant mask and a Boron implant. The implant mask defines the photoresist areas. The Boron implant, which does not penetrate the photoresist, causes the "n" type (NMOS) islands to be doped "p-". This process forms the "p-" area under the gate of the final NMOS transistor. After this step, the photoresist is removed and the entire wafer is exposed to Phosphorus or other "n" type impurity which leaves all islands doped "n-" except those already doped "p-". This later doping step is controlled so the previous "p-" doping of the "n" type (NMOS) islands is unaffected. In an analogous manner, this step forms the "n-" area under the gate of the final PMOS transistor. The oblique view of the CMOS/SOS layout of Figure II-9 helps illustrate the layout of "n" (NMOS) and "p" (PMOS) islands.

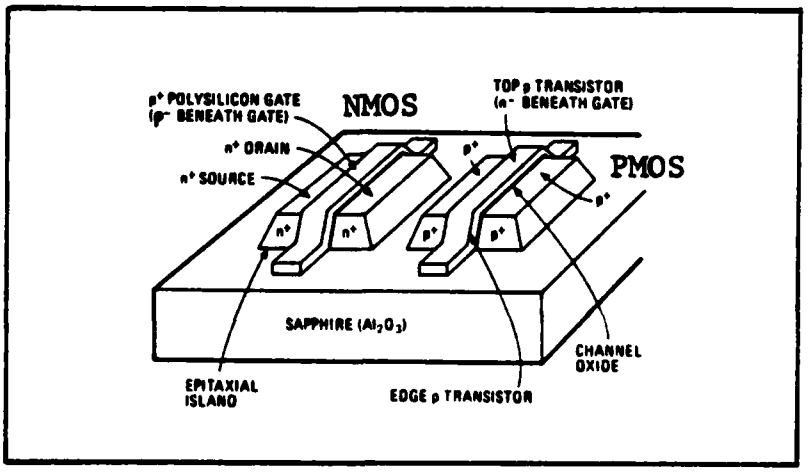


Figure II-9 CMOS/SOS Oblique View [Ref 15:51]

Following these procedures, the islands are oxidized to form the transistor gate oxide. The next step is the formation of the polysilicon layer, doped "n++", which forms the transistor gates. The implant mask is then used twice, once each in its clear field and dark field forms, as a mask for the source and drain diffusions. This self-aligned process leaves the source and drain of the "p" type (PMOS) island doped "p+" while the source and drain of the "n" type (NMOS) island are doped "n+". The remaining fabrication steps are similar to those used in the bulk CMOS and NMOS processes.

CMOS Latch-Up [Ref 10:60-62]

Virtually all MOS devices have undesireable parasitic bipolar transistors. An NMOS device, for example, may form a npn transistor if the "n+" source or drain is negatively biased with respect to the "p" type substrate. Any electrons injected into the substrate could be collected by the other "n+" well if biased positive. The main problem with this type of parasitic bipolar transistor is that it can discharge node voltages, as in pass transistor networks.

The problem of unwanted parasitic transistors is much more pronounced in bulk CMOS circuits, however. In CMOS circuits, there exists the possibility of not only npn parasitics, but also pnp parasitic transistors, thus forming npnp structures. Figure II-10 clearly illustrates a pnp transistor formed by the source of the PMOS transistor, the

"n" type substrate, and the "p" type well of the NMOS transistor. Formation of the npn parasitic, also illustrated in Figure II-10, results from the "n" type substrate, "p" type well, and "n+" doped source of the NMOS device.

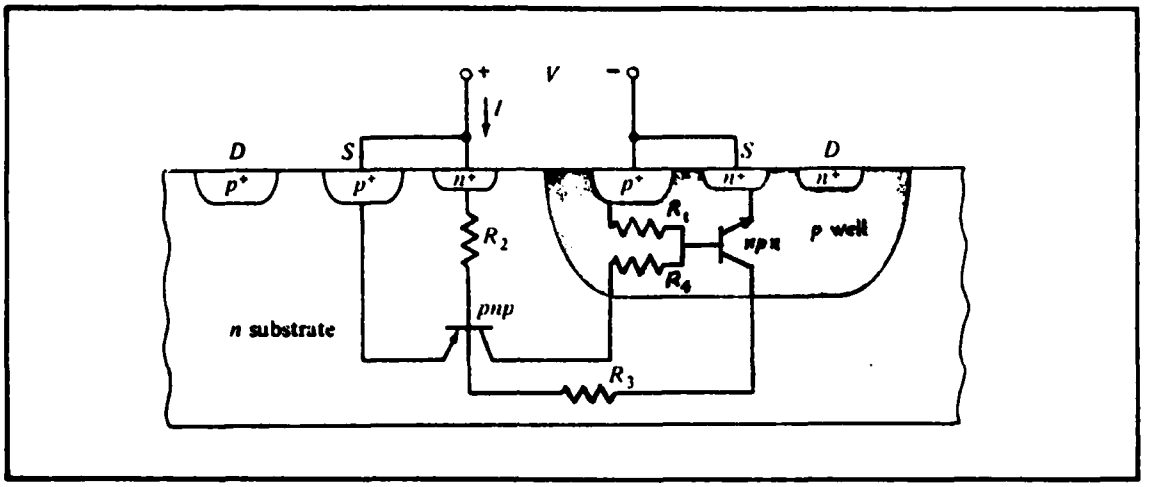


Figure II-10 Parasitic Transistor Model of Bulk CMOS Device [Ref 10:61]

In typical CMOS circuits, these parasitic transistors usually begin to conduct at voltages ranging from 10-20 volts. The magnitudes of the resulting currents are a function of substrate resistance; however, milliampere currents are not unusual. This problem is especially apparent in circuits directly connected to output pins. As power supplies are switched on, transients can easily exceed that required for parasitics to conduct. When this situation occurs, the circuit may latch-up in a particular state and require power-down to reset.

As stated previously, latch-up does not occur with

CMOS/SOS circuits because each individual transistor is isolated by an insulating sapphire substrate. Thus, there is no path for the formation of bipolar transistor currents. The price paid for this elimination of parasitics though, is the formation of MOS edge-transistors on the sides of the "p" and "n" type (PMOS and NMOS) islands. These unwanted transistors are formed wherever gate polysilicon transitions from the sloping island edge to bare sapphire. An undesireable characteristic that the CMOS/SOS designer must be aware of is that these edge-transistors have a lower gate dielectric breakdown voltage than island transistors. Breakdown occurs more easily with the edge transistors because the oxide under the polysilicon gate decreases in thickness toward the island edge (see Figure II-9). This thin oxide is more susceptible to breakdown and does so at relatively small bias voltages. Whereas normal gate oxide may have a breakdown voltage from 50 to 100 volts, edge transistor gate oxide may breakdown from 15 to 20 volts. Because it is usually destructive, the problem becomes critical in circuits that are directly exposed to output pins. Large power-on transients can cause edge transistors to breakdown, thus permanently degrading the characteristics of the island transistor.

One method of reducing the potential for this problem is to use protection circuits on all input pads. A typical CMOS protection circuit, as in Figure II-11, uses diodes which are designed to nondestructively breakdown at a

voltage slightly lower than the gate oxide of the edge transistor. This causes the static charge to be dissipated harmlessly to ground.

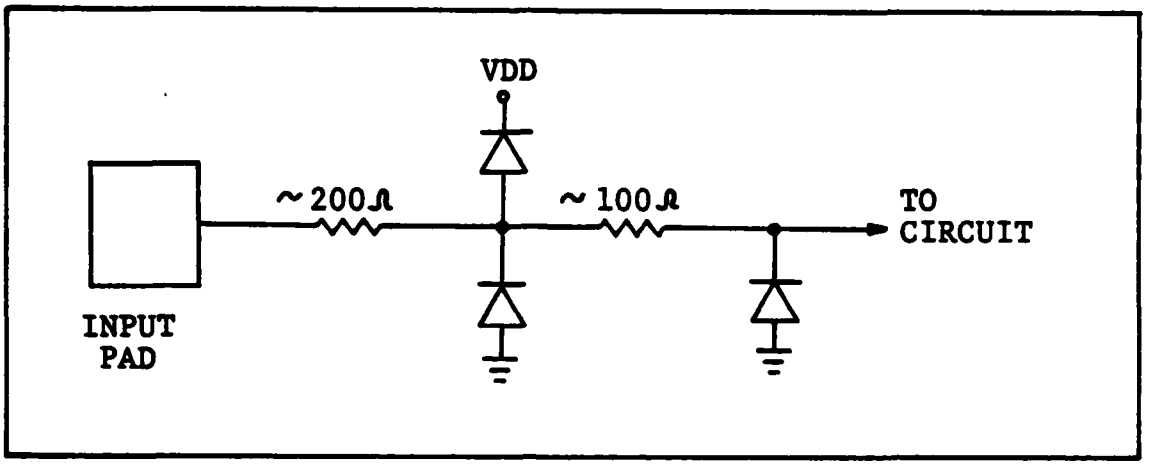


Figure II-11 CMOS Protection Circuit [Ref 10:60]

A second method is to make susceptible transistors circular in shape so that polysilicon does not run off the island edge. Though the Stanford CLL does not directly support circular transistors, they may be layed-out using the CIF RoundFlash command [Ref 16]. This design procedure will not be used in this thesis.

CMOS Capacitance

Four basic capacitances are found in CMOS bulk transistors, whereas CMOS/SOS transistors are characterized by only two. Table II-1 lists most of the contributing capacitances of both bulk and CMOS/SOS devices.

Almost all of the capacitance of the CMOS/SOS device is seen to be between the gate and substrate, which is the

only capacitance necessary for MOS transistor action. Minor gate-drain capacitance is apparent, though it is not as significant as that of bulk CMOS. Bulk capacitances not present in SOS devices consist of side-wall and base drain-to-substrate capacitance and source-to-substrate

Table II-1 Bulk and CMOS/SOS Capacitances [Ref 15:51]

Capacitance Source	Bulk/CMOS	CMOS/SOS	Units
Gate-Substrate	0.25	0.25	pF/mil2
Drain-Sub. (Sidewall)	0.1	--	pF/mil2
Drain-Sub. (Base)	0.1	--	pF/mil2
Gate-Drain	0.04	0.01	pF/mil

capacitance. With silicon-on-sapphire, these capacitances are almost totally eliminated because the island diffusions are driven completely down to the sapphire. Thus, no substrate exists for the formation of base or sidewall capacitances. These, and all capacitances other than gate-substrate, tend to increase power consumption and decrease switching speed since they require a finite charge and contribute to the total time required to charge the gate. The power saving and switching speed advantages of CMOS/SOS over bulk CMOS are obvious due to its less overall capacitance. CMOS/SOS also has the least parasitic capacitance of all current MOS technologies [Ref 15:51].

Design Rules [Ref 8]

The CMOS/SOS design process adhered to in this

thesis uses the same layers as the NMOS process described in Mead and Conway [Ref9]. The only difference the CMOS/SOS designer need be concerned with are the CIF names given to these layers. Table II-2 below lists both the NMOS and CMOS/SOS CIF names for each layer. Before a CMOS/SOS device may be submitted for fabrication, the CMOS/SOS layers of Table II-2 must be substituted for the corresponding NMOS layers.

Table II-2 NMOS and CMOS/SOS CIF Layers

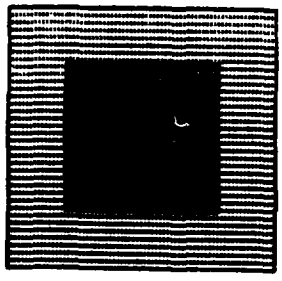
NMOS Layer	CMOS/SOS Layer
ND - Diffusion	SIS - Island
NI - Depl. Mode Implant	SIM - PMOS Implant
NP - Polysilicon	SP - Polysilicon
NC - Contact Cut	SC - Contact Cut
NM - Metal	SM - Metal
NB - Buried Contact	Not Allowed
NG - Overglassing	SG - Overglassing

Fortunately, the similarity between CMOS/SOS and NMOS also extends to the design rules presented in Mead and Conway, but with a few exceptions. Two differences that arise because of manufacturing difficulties are that the butting contact and buried contact are not allowed. Because of the unique arrangement of CMOS/SOS circuits, the butting contact is seldom used anyway. The types of contacts that are allowed are the standard metal-to-poly or metal-to-diffusion via in which a 2L by 2L (L represents lambda, which equals 2.0 microns) is surrounded by 1L of the layer, and a "p" island cut (a cut represents an area which has been etched to a specific layer) where the via is

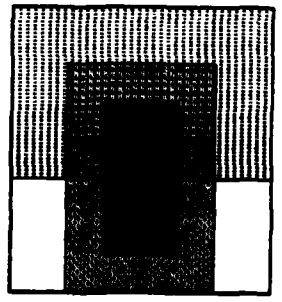
surrounded by 1.5L of implant. See Figure II-12a for an illustration of this type of contact. The implant is necessary to distinguish the cut layer as "p" (PMOS) island rather than "n" (NMOS) island (a cut layer represents the layer at which the etching stops). The CMOS/SOS designer must be aware that all diffusion layers default to "n" (NMOS) island unless surrounded by implant with 1.5L extending past the island edges. Because of its unique four-step implant process, the "n-" channel of the PMOS transistor is only formed in those areas corresponding to implant.

Another type of contact cut that is allowed is a shorting contact between "p" (PMOS) island and "n" (NMOS) island (see Figure II-12b). It resembles the butting contact in that it consists of a 2L by 4L cut surrounded by 1L on all sides by the appropriate layer. In this type of cut however, "p" (PMOS) island material is on one side of the contact and "n" (NMOS) island material is formed on the other with no overlap. This cut is required to short the diode formed between NMOS and PMOS transistors.

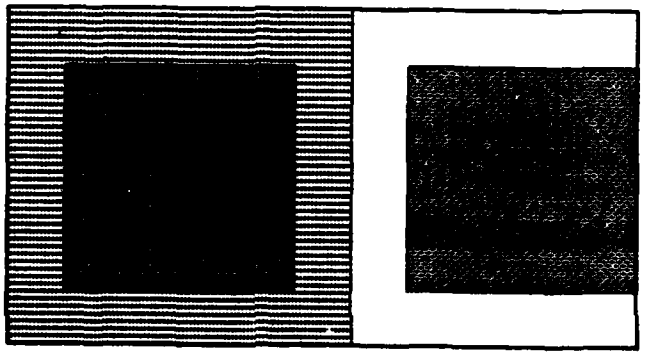
Rules pertaining to island separation require a 3L separation between edges of PMOS and NMOS transistors (see Figure II-12c). Implant used to form PMOS transistors must extend a minimum of 1.5L past the PMOS island edge but must not come closer than 1.5L to an NMOS island edge (see Figure II-12d). Poly used to form transistor gates must extend 2L past island edges, and must not come closer than 2L to an



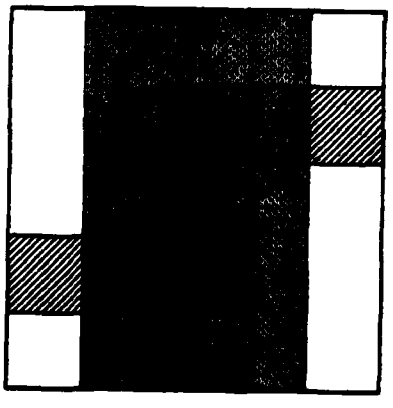
(a) Via Surrounded by 1.5L of Implant



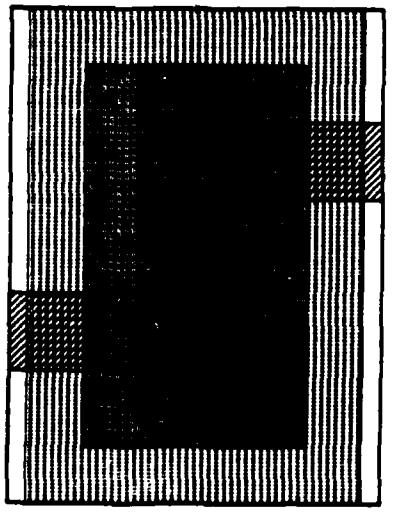
(b) Diode Short Between Islands



(c) P and N Island Separation



(d) Poly Path and N Island



(e) Poly Path and P Island

Figure II-12 CMOS/SOS Design Rules

island edge except when entering or exiting the island area (see Figure II-12e). Additionally, according to notes from Seitz of Caltech, minimum poly-to-poly spacing must also be 2L [Ref 8].

CMOS/SOS Design

The basic concept involved in CMOS/SOS design is to layout PMOS and NMOS transistors so as to best utilize their complementary switching action and, in doing so, conserve power. In many cases, this implies that the typical NMOS designer must discard old approaches and develop entirely new design ideas. CMOS circuits usually do not layout compactly when one attempts to convert a NMOS design to CMOS by brute force. A good strategy for CMOS design is to look for dualities in circuit logic equations. Because of the complementary switching of PMOS and NMOS transistors, they are natural duals. The design and layout of CMOS/SOS circuits will be discussed throughout the remainder of this thesis.

III. Cell and Library Requirements

In order to take advantage of computer aided design tools, a method is required to optimize the placement and routing of components on a chip. At the most basic levels, the designer must arrange fundamental components such as rectangles and wires to implement a design. However, many components of a design occur in regular arrangements that are easily repeatable. The purpose of this chapter is to define and justify the requirements of some of these regular arrangements, called cells. Specifically, the requirements for all basic logic gate cells, an ALU cell, and a CMOS/SOS PLA generator are presented.

Characteristics of Cells

All cells designed in this thesis will be broadly categorized as either standard or general cells, a design method used by semiconductor manufacturers RCA and Mitsubishi [Ref 17:VIII-1-VIII-8,18:828-836]. Standard cells will be classified as those cells which have inputs, outputs, Vdd and ground connections restricted to certain sides of the cell. Also, the Vdd and ground connections will be spaced at specific intervals so that identical standard cells may be tessellated (repeated) vertically or horizontally without the need for external wire connections. General cells will be those cells with no restrictions on connection locations or spacing of external connections.

General cells will usually contain many more components than standard cells and may be partially or completely composed of standard cells or other general cells.

Restrictions on standard cells are necessary to insure proper tessellation of the most basic components of the library. Both space and the designers' time will be saved if all Vdd and ground connections are identically spaced. This relieves the designer from making separate, and frequently error prone, wire connections. The requirement for direct horizontal tessellation is justifiable only for PLA clock-in and clock-out circuits. It is not justifiable for basic logic gates (except for the inverter) because basic gates generally have two or more inputs but only one output. Thus, they cannot be directly connected horizontally.

All cells will be independent of the specific geometry used. Although, the 1982 geometry for CMOS/SOS was 4 microns, the cells will scale accordingly as technology provides further reductions in size. This is possible because all cells are specified in terms of lambda rather than microns, where lambda represents a fundamental distance unit. No geometry or scaling problems will exist with the PLA generator since the geometry will be user established as an input parameter. Currently, however, the geometry for the NMOS PLA generator, PLAGEN, is software coded to 2.5 microns to prevent inadvertent user errors.

As mentioned in Chapter II, the desired

width-to-length ratios of PMOS and NMOS transistor pairs is 2:1. But in chapter 2, it was also noted that the most symmetrical rise and fall times were achieved for ratios of 1.4:1. However, in the interests of ease of design and the desire to comply with industry standards, 2:1 ratios will be used here.

It should be stressed though, that 2:1 ratios will apply only to transistor pairs, not to such circuits as multiple input NAND and NOR gates which have several transistors in series and parallel. Although this situation is discussed in detail in Chapter V, the problem with NAND and NOR gates is that the combined delay from individual series transistors is greater than that of the transistors in parallel. Thus, 2:1 ratios tend to produce asymmetrical responses. Therefore, the only requirement for these types of cells is that their respective ratios produce symmetrical responses and with approximately the same delay for identical gate families. This requirement is necessary so that all stages of a combinational logic design will produce similar response statistics.

All clocking will be accomplished by means of a two-phase non-overlapping clock signal. All cells that require clocking will receive the clock signals from sources external to the cell. The two-phase clock is usually generated on-chip within a clock-in pad, but pads will not be designed as part of this thesis.

Library Requirements

The basic cell library must contain the most commonly used components of a specific technology. For example, the Stanford NMOS cell library contains an assortment of pads, superbuffers, and various computational components and support cells [Ref 4]. Some of these cells, such as the computational elements, translate directly to CMOS technology. Others, such as superbuffers, are unnecessary for CMOS designs for reasons discussed in Chapter II. Instead, to improve voltage transfer characteristics and noise margins, CMOS circuits often have double buffered outputs. Double buffering requires the addition of two series inverters on circuit outputs, each with successively larger W/L ratios, and aids in driving off-chip loads [Ref 10:106].

Basic logic gates are the building blocks of most technologies, and CMOS/SOS is no exception. As such, the CMOS/SOS INVERTER, NOR, and NAND gates will be layed out as standard cells. The NAND gates will require multiple inputs in addition to the standard two input gate. Multiple input gates will be required to simplify the layout of the ALU. Also, the CMOS double buffered output will be layed out as a standard cell.

These standard cells will be required in order to implement a bit-slice ALU as a general cell. The bit-slice ALU will be iterated to form a four bit ALU that will have the capability of being stacked to form ALUs with word

lengths equal to integer multiples of four bits. The 4-bit ALU will have the specifications listed in Table III-1.

Table III-1 ALU Requirements

INPUTS	OUTPUTS
1. One 4-bit opcode	1. One 4-bit result
2. Two 4-bit operands	2. One bit carry-out
3. One bit carry-in	
4. One bit function select	

Since a four-bit opcode plus a function select will be used, a total of 16 arithmetic and 16 logical functions will be implemented. ALU clocking will be accomplished by means of two-phase, non-overlapping clock signals. An internal clocking scheme will be required to propagate operands on a particular clock phase.

Other required standard cells will include PLA clock-in and clock-out circuits and a transmission gate to accomplish general clocking. The PLA clock-in and clock-out cells will be required to butt directly to PLA inputs and outputs respectively and tessellate horizontally without requiring additionally connections. The clock-in cell will provide both a complemented and uncomplemented input, but the clock-out cell will provide simply a non-inverted clocked output. The transmission gate will be designed as a separate cell, and will require both a complemented and uncomplemented phase of the two phase clock signal (either phase one or phase 2).

CAD Tools

Library cells will be required to be compatible with most CLL commands and constructs. However, before fabrication will be possible, the CIF file produced by CLL will have to be edited to provide the correct CMOS/SOS layers. The main differences will be that the buried and butting contacts will not be used, and that the implant layer will represent those areas forming PMOS transistors rather than depletion mode transistors. The design rules specified in Chapter II will apply to all general cells but will not necessarily apply to all standard cells.

Other software tool requirements are based largely on proposed modifications to the NMOS PLA generator, PLAGEN, which will be modified to generate the CMOS/SOS PLA. The PLA, which may also be considered a general cell, will be composed of NAND planes rather than the standard AND and OR planes. One NAND plane will form the product terms and the other will form the sum of product terms. Unlike the NMOS PLA, which uses NOR/NOR planes, the outputs of the CMOS/SOS PLA will not require complementing. The CMOS/SOS PLA generator will have the following features:

1. A maximum combination of 200 inputs and outputs but no limit on the number of output terms (other than that imposed by hardware constraints). It should be noted that a N-input PLA reaches a limiting case when it has 2^N product terms, at which point it is equivalent to a Read Only Memory. However, the PLA is most effective as a replacement

for logic gates when the number of product terms is much less than 2^N.

2. All options currently included in PLAGEN will be eliminated because they do not apply to CMOS technology. For example, the "-o" option omits pull-up transistors on the OR plane of the NMOS PLA. CMOS technology, however, does not use passive pull-ups. Similarly, the "-c" option complements inputs so that afterburners may be used, but afterburners are unnecessary for the CMOS/SOS PLA. The "-g#" option sets the frequency of ground busses so that a ground buss is connected every "#" product terms. The "-i" option interleaves inputs. Neither of these options will be used for similar reasons. [Ref 3]

3. Options will be added to allow automatic clocking of inputs, outputs, or both inputs and outputs by means of the PLA clock-in and clock-out standard cells. Clocking will be accomplished by means of a two-phase non-overlapping clock signal. Inputs will be clocked in on phase 1, and the result will be available on phase 2.

4. The PLA pieces will be defined as portions of the NAND planes. Their external definitions and CIF files will reside in directories accessable by all AFIT CAD users. The PLA pieces will not necessarily adhere to all CMOS/SOS design rules. However, when the pieces are combined in the PLA, all CMOS/SOS design rules will be met.

5. The input will be of the same form as that of the NMOS PLA generator. The only difference will be the

specification of 4 micron geometry rather than 2.5 micron geometry, and that NMOS options will not be allowed.

6. The output will be a CIF file containing external reference records for the CIF loader, calls to PLA pieces, and an identification line including the PLA symbol. The output file will contain only references to the standard NMOS layers. The CIF file will be ready to be processed by CLL to produce a plot or another CIF file. It will then be necessary to edit the original CIF file so that CMOS/SOS layers are introduced. Additionally, two lines will be sent to the users' terminal containing CIF bounds coordinates and input verification. Error conditions will also be detected, and appropriate responses will be sent to the users' terminal.

7. The PLA generator will be written in the "C" language, and will be compiled on the VAX/11-780. It will be compatible with other UNIX (or UNIX compatible) systems.

Documentation

In addition to the descriptions of the library cells in the text of this thesis, each cell will be separately documented in the appendices. The format in Table III-2 will be used for the documentation of each cell.

The CMOS/SOS PLA generator will have complete software documentation as well as appropriate Structure Charts for each module. A brief users' guide similar to that of the NMOS PLA generator will be included in the

appendices. Additionally, sample PLAs will be documented with all appropriate nodes and connections labled. The method required to convert CIF NMOS files to CIF CMOS/SOS files will also be documented.

Table III-2 Documentation Requirements

1. Name and CIF ID
2. Logic symbol (Standard cells only)
3. Circuit Diagram (Standard cells only)
4. One line description
5. Physical properties
   (a) Size
   (b) Interface requirements
   (c) Estimated power consumption (to be determined by SPICE analysis for all standard cells and estimation for all general cells)
6. One paragraph description
7. Operation (ALU only)
8. CIFPLOT with all inputs, outputs, Vdd and ground nodes and coordinates labled.

Interface Requirements [Ref 10:293-298]

Two types of interface requirements must be addressed; on-chip and off-chip interfacing. As previously discussed, on-chip interfacing will be facilitated by the use of properly documented standard cells as basic building blocks. All connections will be marked to include coordinates (with respect to the cell origin), width of the connection, and layer.

Off-chip interfacing requires an examination of the system to be interfaced. Usually, digital systems are constructed using only one logic technology such as CMOS, NMOS, or TTL. Occasionally however, it is more advantageous

to combine different technologies into a single system. For instance, TTL and NMOS systems with large memory requirements often use CMOS memories to reduce overall power consumption.

Since TTL is the most widely used form of digital IC, only CMOS to TTL interface requirements are specified. If Vdd levels of 5 volts are to be used, direct interfacing will be possible. However, it is generally advisable to use double buffers on circuit outputs to enhance the CMOS circuits' ability to source TTL gates. Additionally, an external pull-up resistor is normally used to ensure symmetrical voltage swings. Operation of the CMOS circuit above 5 volts will require a diode clamp at the TTL input to prevent excessive voltages and subsequent damage to the TTL circuits.

IV. Library System Level Design

Various methods of implementing the ALU and CMOS/SOS PLA requirements are investigated. Circuit level diagrams of the proposed ALU and PLA are also presented. The design of the ALU, based upon the full adder circuit, uses four full adders and sequential logic as well as additional combinational logic. The circuit diagram of the PLA illustrates the general arrangement of a CMOS PLA. A structure chart of the CMOS/SOS PLA generator is also presented. Standard library cells are not discussed, as their design is relatively fundamental. Standard library cell layout, as well as detailed designs of the ALU and PLA generator, will be presented and discussed in Chapter 5.

ALU Design

Most commercially available ALUs are implemented in simple combinational logic, while at least one university developed ALU is based upon selector logic circuitry [Ref 4,19:4-6]. Another method uses multiple stages of flip-flops, usually J-K flip-flops, to implement both combinational and sequential logic portions of an ALU [Ref 20:333-339]. This type of ALU is capable of performing various operations that may require the sequential shifting of bits, such as that involved in multiplication and division as well as serial addition. It has the disadvantages of requiring a complex clocking scheme and

does not encourage a highly regular layout. The other two methods also provide unique advantages as well as disadvantages.

The selector logic ALU is much more general in that it uses a grid of polysilicon paths crossing diffusion paths to generate functions. For the NMOS selector circuit, selectively located enhancement mode transistors determine which inputs are to be propagated, based upon a particular opcode. A PLA is usually used to generate appropriate opcodes for different functions. To implement various other functions, it is only necessary to change the PLA. If CAD tools are available, this procedure is rather simple. One serious disadvantage however, especially for CMOS, is the design complexity of the selector logic circuitry. Whereas simple pass transistors are used in a NMOS selector circuit, the CMOS design requires both NMOS and PMOS transistors in a regular arrangement so as to accomplish complementary switching. In addition to increasing the size of the selector circuit, and unlike the NMOS version, both Vdd and ground must be supplied.

Simplicity of design is a primary advantage of combinational logic but tends to restrict a design (in particular, an ALU) to a set of unchangeable operations. To generate other functions, the circuitry of the ALU must be changed or more circuitry must be added. However, to take full advantage of the standard and general cell approach of the proposed CMOS/SOS cell library, the requirement exists

to be able to use predefined cells in a repeatable and regular arrangement. This type of modular approach is best suited to a ALU which uses combinational logic to perform all arithmetic and logical functions, and which uses simple clocking circuitry.

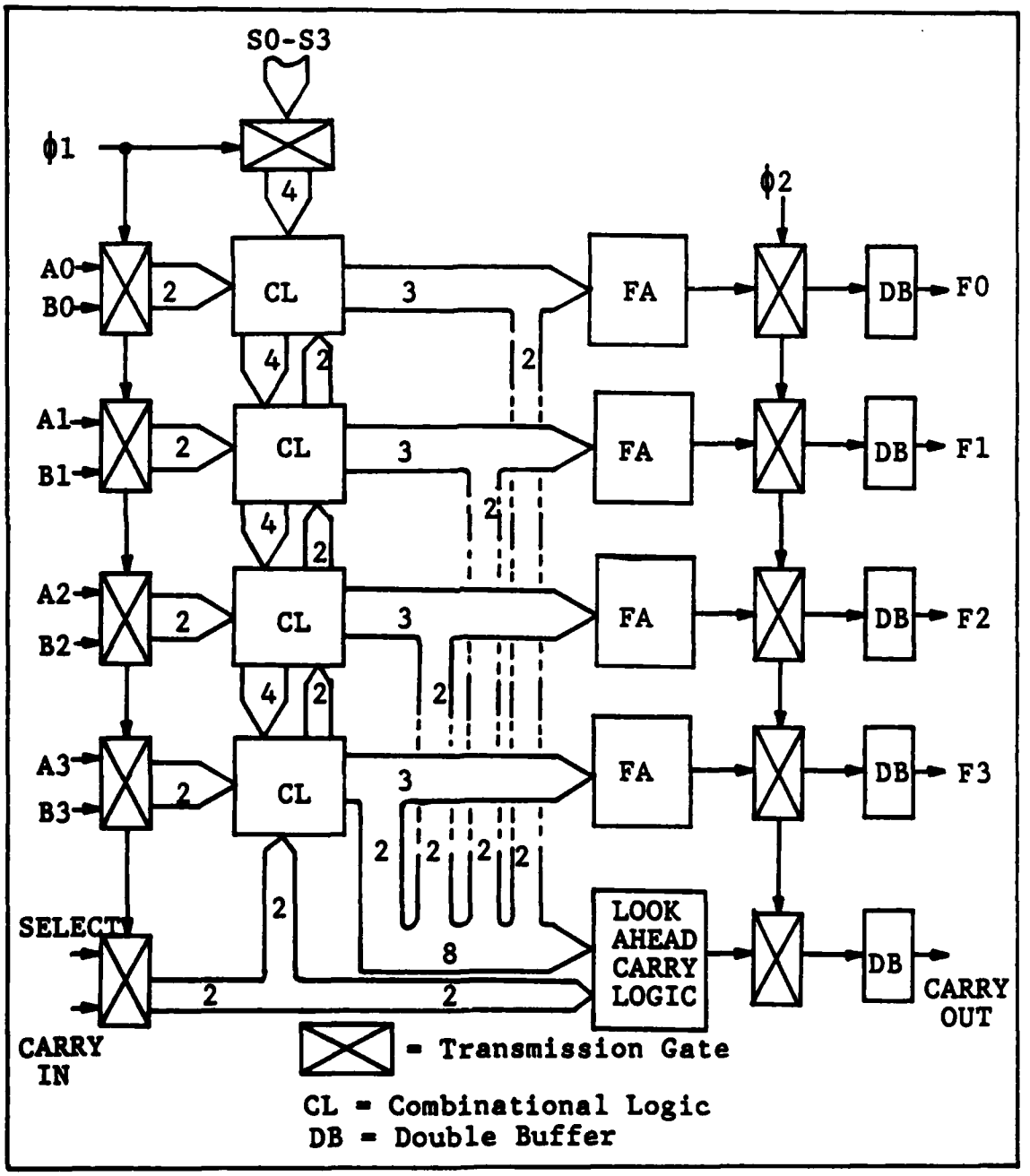


Figure IV-1 4-Bit ALU Block Diagram

A block diagram of the proposed ALU, a modified version of Motorolas' MC10181, is illustrated in Figure IV-1 [Ref 19:4-6]. Each bit slice consists of a full adder, other combinational logic, and operand as well as opcode and output transmission gates. The transmission gates are used to pass data on a specific clock phase. All data must be entered into the ALU on phase 1, ensuring that all outputs are available on phase 2. Carry function logic is not part of each bit slice since full internal look ahead carry is utilized.

Several tradeoffs were made during the decision to implement the look ahead carry technique rather than the ripple carry technique. The latter would have made it possible to eliminate all additional combinational logic not incorporated into the basic bit slice. The carry-out from each bit slice would merely connect to an input of each successive stage. However, the main problem with this type of implementation is the delay associated with ripple carry. Since each bit of the output of the ALU would depend on the value of the input carry bit, the highest order output bit would not be at its final state until the carry had propagated through all bit slices. In large ALUs, this delay can become a considerable limitation.

The look-ahead carry technique has the advantage that all function output bits as well as the carry-out bit are available at the same time. The only delay introduced is the minimum delay required to generate any single output

bit. Though dependent on the number of stages of combinational logic used, the delay factor introduced is much less than that associated with ripple carry. As previously stated, the main disadvantage is the slight, but tolerable, irregularity of the design. This problem will make it necessary to add extra combinational logic any time that bit slices are tessellated to form multi-bit ALUs. The better solution will be to combine four bit slices to form a 4-bit ALU, and then iterate the 4-bit ALU. As stated in Chapter III, this procedure will make it possible to form word lengths equal to integer multiples of four bits.

PLA Design

The CMOS/SOS PLA is similar to the NMOS PLA only in that two planes, one rotated 90 degrees, generate outputs that are sums of product terms. The internal structure of each plane is considerably different. An examination of the PLA circuit diagram of Figure IV-2 reveals that both planes are NAND planes and that Vdd and ground busses are opposite those of the NMOS Pla. Additionally, each row of product terms requires one row of NMOS and one row of PMOS transistors rather than simply one row of NMOS transistors. An analogous situation occurs for the columns forming the sum of products. This particular arrangement was found to be the most advantageous because it eliminates the requirement for inverters at the PLA outputs and maintains the standard practice of using PMOS devices as pull-ups.

Although the circuit appears somewhat unusual and does not employ the standard AND/OR plane configuration, the output is identical to that of an AND/OR PLA. For this reason, and to simplify explanations, the PLA planes will henceforth be referred to as "AND/OR" planes.

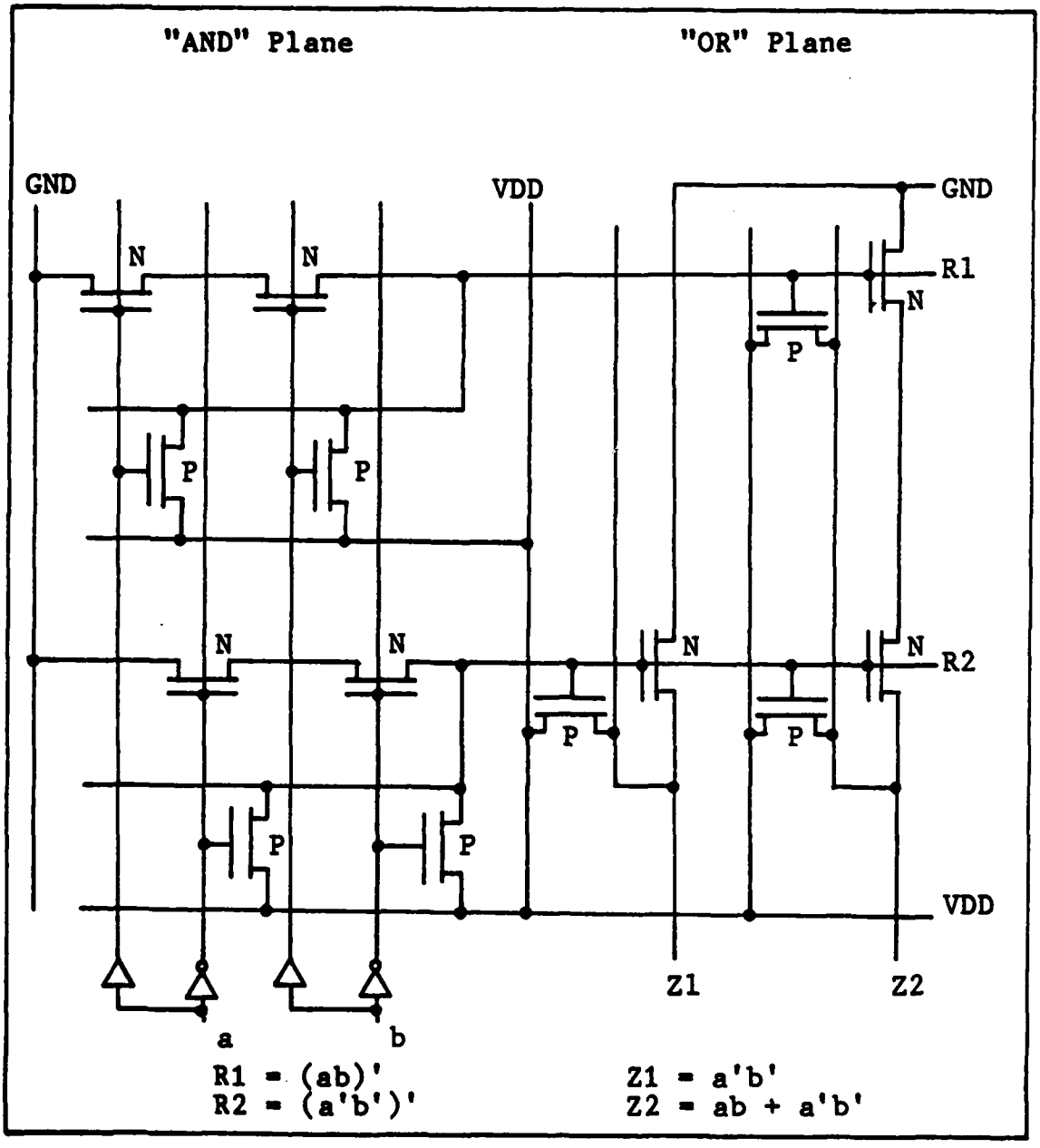


Figure IV-2 2x2x2 CMOS PLA Circuit Diagram

As an example of the PLA operation, consider the case where the inputs "a" and "b" are both low. In the "AND" plane, since the inputs are both inverted, the lower two NMOS transistors are switched on while the lower two PMOS transistors are switched off, pulling product term R1 to ground. In the "OR" plane, the reverse situation occurs. The NMOS transistors are off, but the PMOS transistors conduct and pull result Z1 to Vdd. Analogous input conditions result in the PLA output for Z2 as shown in Figure IV-2.

CMOS/SOS PLA Generator [Ref 16]

The purpose of the PLA generator is to transform a truth-table-like input file into a file formatted in CIF. This file may then be processed by CLL into a file that may be used to generate a plot or fabricate a working PLA. The former process may be accomplished by the CIF "C" command which is used to call a specific symbol (such as a PLA cell) and to specify a transformation that is applied to all geometry contained in the symbol definition. The call command, which will be the primary CIF command to be used, identifies the symbol to be called by a symbol number. The symbol numbers must be assigned to pieces of the PLA planes, represented schematically in Figure IV-2, so that when they are called and transformed appropriately, a complete PLA will be generated. Breakdown of the CMOS/SOS PLA into the various pieces will be discussed in Chapter V.

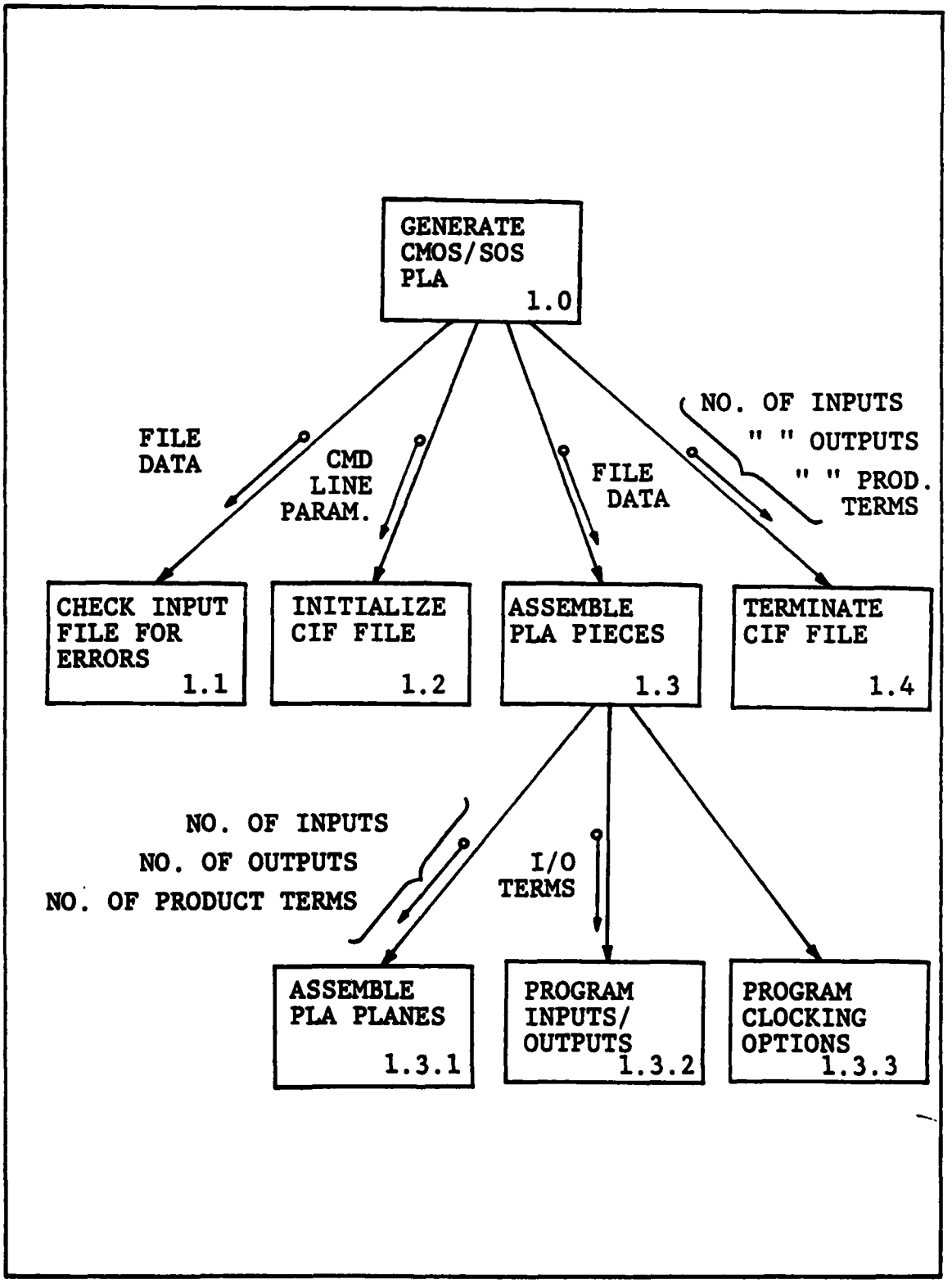


Figure IV-3 PLA Generator Structure Chart

The main problem though, will be to manually draw a large PLA to scale, and then use CLL to layout the parts of the PLA that are easily repeatable. A high level structure chart of the software requirements is illustrated in Figure IV-3.

As the chart illustrates, the PLA generator will consist of basic input file error checking routines, routines to initialize and terminate the CIF file, and routines to generate and program the required functions. Initializing the CIF file requires writing external definitions of all PLA cell symbols for the CIF loader, and a definition of the PLA symbol and lambda (in hundredths of microns). Termination of the CIF file merely requires that the CIF Finish Command "DF" be written as the last statement of the file and that CIF bounds coordinates be written to the user terminal. By far, the largest routines are those that generate the AND/OR planes and program the product and sum of product terms. Through interpretation of the input file data (the command line and subsequent ones, dashes, and zeros), these routines determine which symbols to call and the necessary transformations. Detailed designs of all library components, as well as the CMOS/SOS PLA generator, are presented in Chapter V.

V. Library Detailed Design

Detailed designs of all library components and the PLA generator are presented in this chapter. SPICE and design rule analyses of the PLA and standard cells are also discussed. Standard library cells are shown in both their schematic forms and actual CLL layouts. The 4-bit ALU is illustrated at the logic gate level with all inputs, outputs, and clocking shown. Individual logic gates of the ALU are cross-referenced to the corresponding standard library component. A sample PLA in addition to all PLA cells is also layed out in final form. Additionally, individual modules of the PLA generator are broken down into their appropriate structure charts, and their individual functions are discussed.

Standard Cell Design

Detailed designs of standard cells were accomplished in two steps. First, schematic representations were established, and secondly, the cells were layed out according to the requirements established in Chapter III. Standard cells were layed out as part of the detailed design because they are required for ALU implementation and also, because they will aid the reader in visualizing layouts as they are discussed. All standard cell and PLA cell layouts are represented by CIFPLOTs in Appendix B (CIFPLOTs are similar to CLL plots but have much denser stipple patterns

and are thus, more aesthetically appealing). In all, a total of seven standard cells, not including PLA cells or PLA clock-in or clock-out cells, were designed and layed out. Each is described in the following subsections.

Inverter The first cell designed was the basic inverter shown schematically in Figure II-1 of Chapter II. Two implementations were made, with the final layout shown in Figure V-1. Upon examination of the

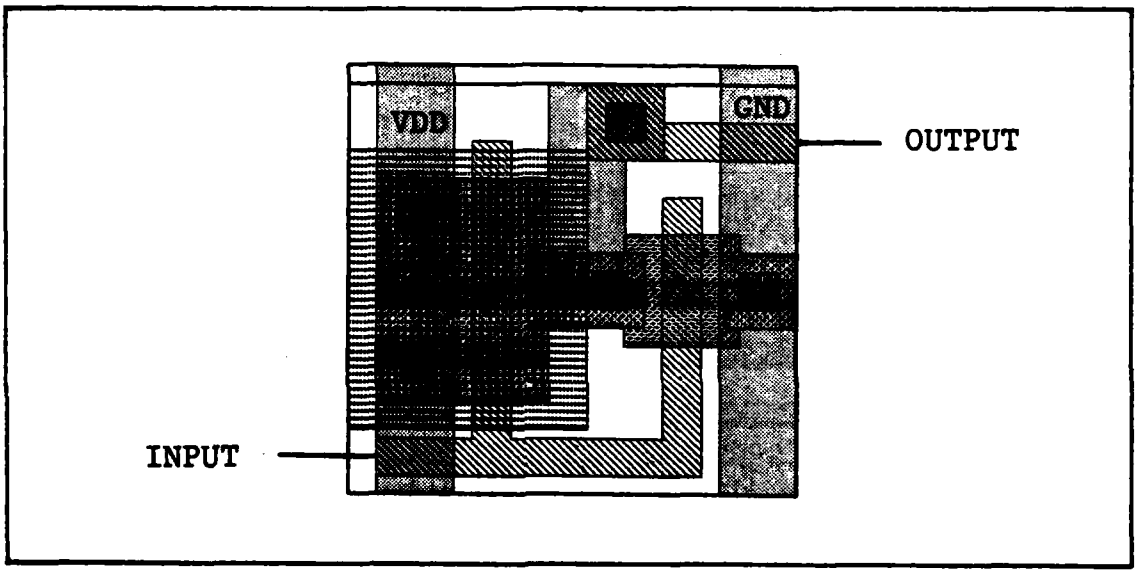


Figure V-1 CMOS/SOS Inverter Layout

inverter layout, it becomes obvious that the cell meets the requirements for vertical tesselation set forth in Chapter III. However, vertical tesselation ,as opposed to horizonal tesselation, resulted in an inverter that was relatively large, with some wasted chip space. Consequently, to provide more flexibility for future designs, the original, smaller layout is also included in the standard cell library and may be examined in Appendix B. Although 2:1 ratios were

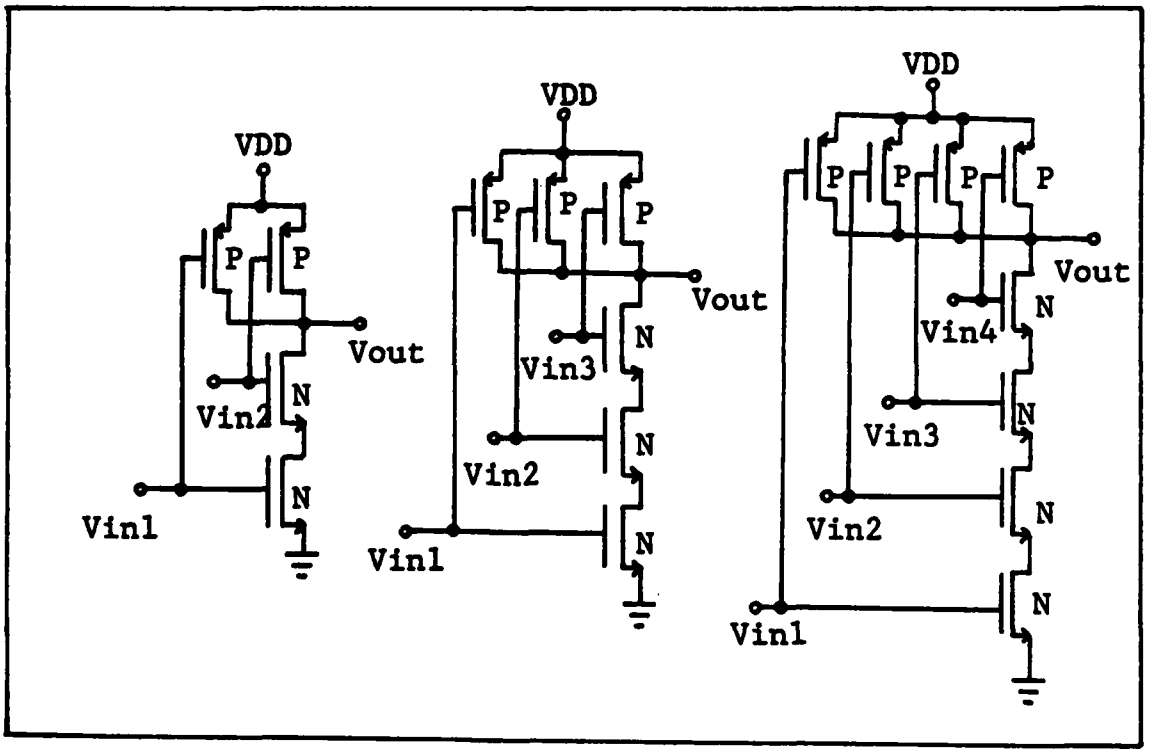
used for both inverters, the layout of Figure V-1 uses larger gate widths (PMOS = 12um NMOS = 6um). It switches at approximately the same rate as all NAND cells. The other inverter uses minimum 2:1 ratio CMOS/SOS geometry (PMOS = 8um NMOS = 4um) and thus, is somewhat slower.

Before introducing other standard cells, a few words about CMOS/SOS layout may prove helpful to future designers. At first glance, the implant surrounding the PMOS transistor may appear excessive. Those designers familiar with NMOS will recall that implant need only extend 1.5 lambda past the intersection of polysilicon (red) and diffusion (green). For the CMOS/SOS inverter design however, this would result in an unwanted (and potentially damaging) diode where the implant stops but diffusion continues. The only place this is acceptable is where a 2x4 cut, surrounded by 1 lambda of layer, is used to short the diode (see Figure II-12a). In Figure V-1, this cut is positioned at the center of the cell.

Another potential problem area arises from the contact cut itself. The natural inclination for NMOS designers is to run a diffusion output from the contact cut location. This practice will once again result in an unwanted diode, or at best, design rule violations. The designer must remember that diffusion intersected with implant results in a p island, and that diffusion intersected with <u>not</u> implant results in a n island, and that island separation <u>must</u> be 3 lambda. The easiest solution

for obtaining an output from the cut location is to surround the cut with metal and run the output out as metal. Where necessary, the metal may then be changed to polysilicon by using an ordinary via. All cells, except for the three and four input NAND gates, use this method. Alternatively, individual cuts may be made to each island, and each island may then be connected with metal. The three and four input NAND gates use this island type layout method.

NAND and NOR NAND gates with from two to four inputs were layed out in a manner similar to that used with the inverter. The NAND gates, represented schematically in Figure V-2a-c, are all exact duals of identical input NOR



(a) 2 Input NAND (b) 3 Input NAND (c) 4 Input NAND

Figure V-2

gates. In fact, if PMOS and NMOS transistors are interchanged ,and if the Vdd and ground lines are reversed, the NAND gates become NOR gates. NAND gates are prefferred over NOR gates however, because the NOR is inherently slower. Analysis of the two input NOR of Figure V-3 reveals that the NOR gate has two PMOS transistors in series. Conversely, the two input NAND gate of Figure V-2a has two NMOS transistors in series. The resitances and delays of both types of transistors add in series, causing the resultant delay to be greater than that of a single transistor. Since the delay of the PMOS is approximately twice that of a NMOS transistor (because hole mobility is approximately half that of electron mobility), significant delays are introduced if PMOS devices are connected in series. The worst delay becomes apparent when both NOR inputs are low, causing both PMOS gates to switch simultaneously on.

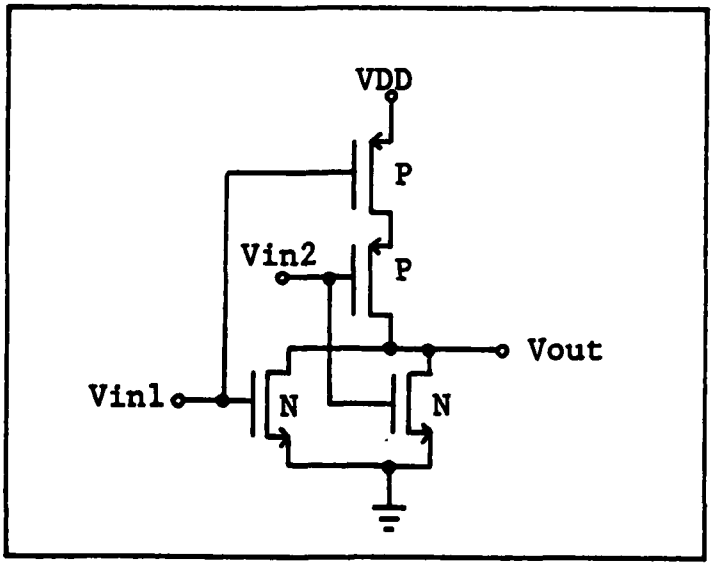


Figure V-3 CMOS NOR Gate

The desired method of eliminating this problem is to increase the width-to-length ratio of the PMOS gates so that their combined gate delay is approximately equal to the NMOS gate delay for all input conditions. Although this solution is acceptable, it obviously results in a much larger layout. CMOS layouts are already inherently larger than other logic families because they require two transistors where, for NMOS and other technologies, only one is required. Increasing PMOS areas only increases the entire cell area, which results in other delays caused by increased parasitic capacitances and by the distances signals must travel. For this reason, only the two input NOR gate was designed.

It is interesting to note the width-to-length ratios of all three NAND gates. As would be expected, a problem similar to that of the NOR gates exists because of the NMOS pull-down transistors being in series. As a result, their delay response adds in series much like the PMOS transistors of the NOR gate. Additionally, the resistance of each gate is another parameter that adds in series to provide an overall greater pull down resistance. This series resistance and the capacitance of the load form an RC time constant which determines the delay. Thus, as the RC time constant becomes greater due to the increased resistance of series gates, larger width-to-length ratios for the NMOS transistors are required to counteract the delay. This problem results in larger layouts, but since NMOS transistors have inherently less delay than PMOS

transistors, it does not result in layouts as large as those required by NOR gates. For the NAND gates of the standard cell library, the ratios were adjusted to provide approximately symmetrical responses according to the number of inputs, and according to the various permutations possible for input conditions.

These ratios were determined by an iterative method using SPICE (see Appendix C) and the P and N MOSFET models for the inverter used in Chapter II. Best case as well as worst case analyses were made for each multiple input gate. In considering the 4 input NAND, SPICE simulations were made for the condition where all inputs changed simultaneously and also where only one input changed. These two conditions tested the best case pull-up situation, where all four PMOS gates act in parallel to source the load, and the worst case situation where only one PMOS transistor sources the load. These results were compared to the pull-down delay, which was constant for all inputs, and a compromise was made in determining gate widths which produced the most nearly symmetrical responses for the two conditions.

After many iterations involving most standard cells, an optimum transitional delay of approximately 6 nsec was arrived at for a 0.1 pF load, the equivalent of a fan-out factor of from 5-10 depending upon the capacitance of the cell. Attempts were made to make all high-going as well as low-going delays equal to, or symmetrical about, this time period. For example, the four input NAND gate of Appendix B

required NMOS gates that were 30 microns wide and PMOS gates 8 microns wide, for a width-to-length ratio of 1:3.75. All channel lengths were maintained at the minimum possible of 4 microns. Analogously, the three input gate uses ratios of 1:3 (8/4:24/4) and the two input gate uses ratios of 1:1.5 (8/4:12/4). The NOR gate ratio was 5.5:1 (24/4:4/4). An examination of the various SPICE simulations of Appendix C justifies these ratios. As noted in Chapter III, 2:1 ratios simply do not produce desireable results for multiple input gates.

A problem associated with providing symmetrical ratios however, is a tradeoff between the reduction of actual gate delay and an increase in overall circuit delay due to the greatly increased size of layouts and added parasitic capacitances of extra connections. Since CMOS/SOS is desireable primarily for its speed advantages, a compromise situation must be achieved.

Operation of the NAND gates is straightforward. If any input is low, the corresponding PMOS gate conducts, and the output is tied to Vdd. Because the NMOS gates are connected serially, the output can become low only when all inputs are high. The NOR gate operates similarly and produces a high output only when all inputs are low, causing the two series PMOS transistors to conduct.

The number of NAND gate inputs was limited to four because of a characteristic unique to CMOS technology. That is, when a CMOS device has several inputs, its transfer

characteristic changes depending on how many of its inputs change values. To illustrate this property, transfer curves for a 4 input NAND gate are shown in Figure V-4. These curves show that the characteristic for the simultaneous change of all four inputs is significantly different than that caused by the change of only one input. This is because all MOSFETs of a CMOS cell have nearly equivalent resistances while in the conductive state. Thus, as mentioned previously, with all inputs of the 4 input NAND in the low logic state, the combined resistances of the parallel PMOS gates is considerably less than when one gate is switched low. The situation is unlike that of a static MOS cell in which every driver must have a much lower impedance than the load in order to achieve a sufficiently large voltage swing. Because of this shift in the transfer curve, noise immunity decreases, thus, limiting the usefulness of NAND gates with more than 4 inputs. An analogous limitation exists with NOR gates. [Ref 21:203-206]

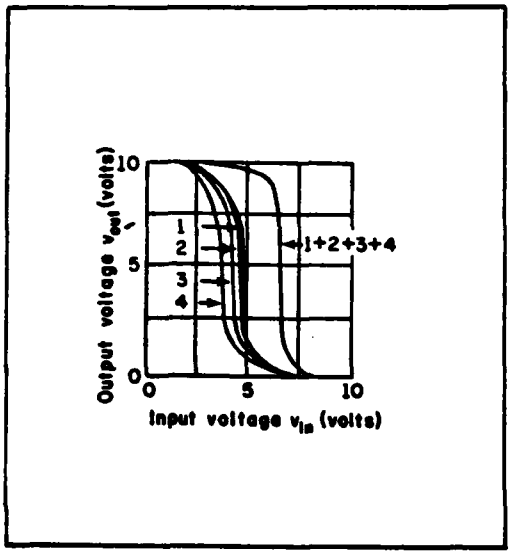


Figure V-4 Transfer Curves of 4 Input NAND Gate [REF 21:205]

Transmission Gate The only way to effectively clock CMOS circuits is by means of the CMOS transmission gate, shown schematically in Figure V-5. It conists of a

NMOS/PMOS transistor pair with common sources and drains. The clock signal, in both its inverted and noninverted forms, is applied to the transistor gates as shown. When the clock signal is high, both gates conduct and the input is propagated to the output. When the clock signal is low, both gates switch low, and the input is effectively cut off

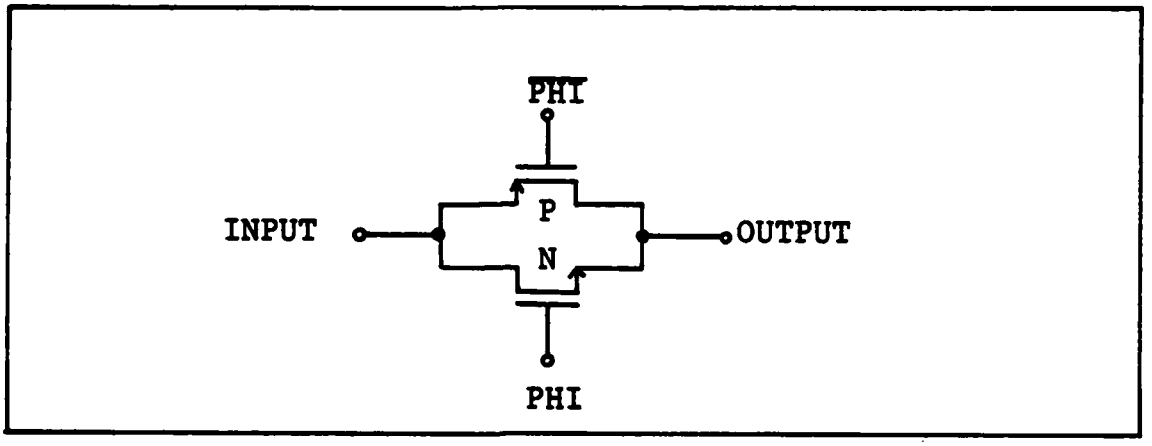


Figure V-5 CMOS Transmission Gate

from the rest of the circuit. A unique property of the transmission gate is that it propagates signals equally well bidirectionally. This particular transmission gate is included as a subcell in the PLA clock-in cell.

SPICE analysis of the transmission gate did not provide expected results, probably because the circuit models were for bulk MOSFETS rather than true transistors on insulator. The problems arose from the difference in NMOS and PMOS bulk voltages (NMOS bulk is at ground and PMOS bulk is at Vdd). A voltage divider resulted, limiting transmission gate output to Vdd/2. The final results in Appendix C required the addition of an external resistive

load to offset the voltage divider. Nevertheless, an ideal simulation was not achieved because the resistive load resulted in an increased RC time constant and greatly increased pull-down delay. Hence, usefulness of the transmission gate may be questionable. Physical testing of a fabricated device may be required to verify operation.

Double Buffered Output Double buffered output cells are the largest of all the standard cells, with cell dimensions approximately 100x80 lambda. The circuit diagram of Figure V-6 shows approximate gate dimensions. Extremely

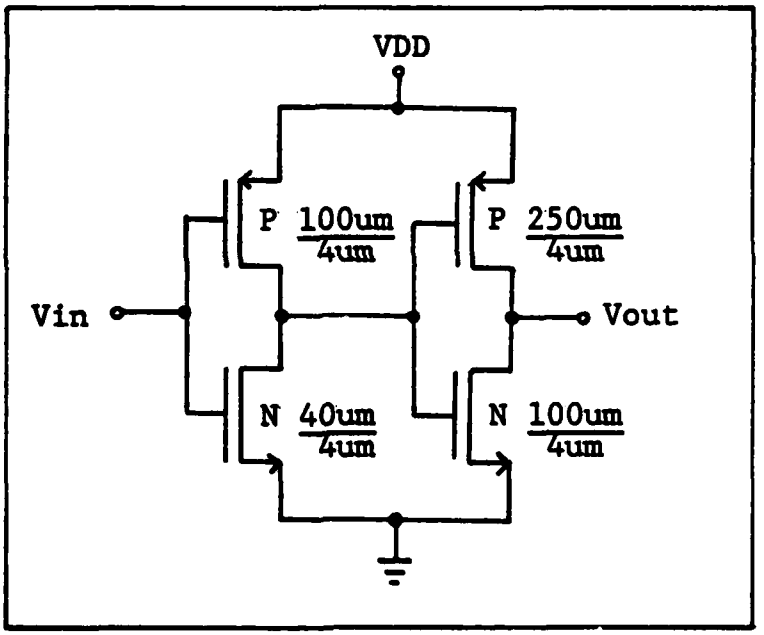


Figure V-6 CMOS Double Buffered Output

large gate widths were used to improve voltage transfer characteristics and noise margins. This enables the CMOS/SOS circuit to drive large off-chip loads of approximately 15 to 20 pF as well as TTL LSI devices. Since the largest gate length was 250 microns for one of the PMOS

transistors, the layout required a clever scheme to prevent an inefficient use of chip space. Hence, the largest gates were layed out in a serpentine manner much like a diffused or thick film resistor. The gate widths for the double buffered output are about the same as the dimensions given for the 4000B and 74C CMOS series of integrated circuits as specified by Hodges and Jackson [Ref 10:107]. Every output of these series of devices is double buffered and is specified as being capable of driving one TTL series 74LS input.

The double buffered output cell simulated as expected, with characteristic sharp pull-up and pull-down transitions (see Appendix C).

ALU Design

The four bit ALU will use all of the standard cells as described in the previous section, with the exception of the NOR cell. Its logic gate representation is shown in Figure V-7, and as previously stated in Chapter III, was derived from the Motorola MC10181 which is based largely upon the full adder circuit. Of course, other combinational logic provides the look ahead carry feature. The main difference between this design and the Motoral ALU is that it uses only NAND gates and inverters and has clocked inputs and outputs as well as double buffered outputs. The "P" and "G" outputs are part of Motorolas' design which allows the use of an external look ahead carry circuit for ALUs with

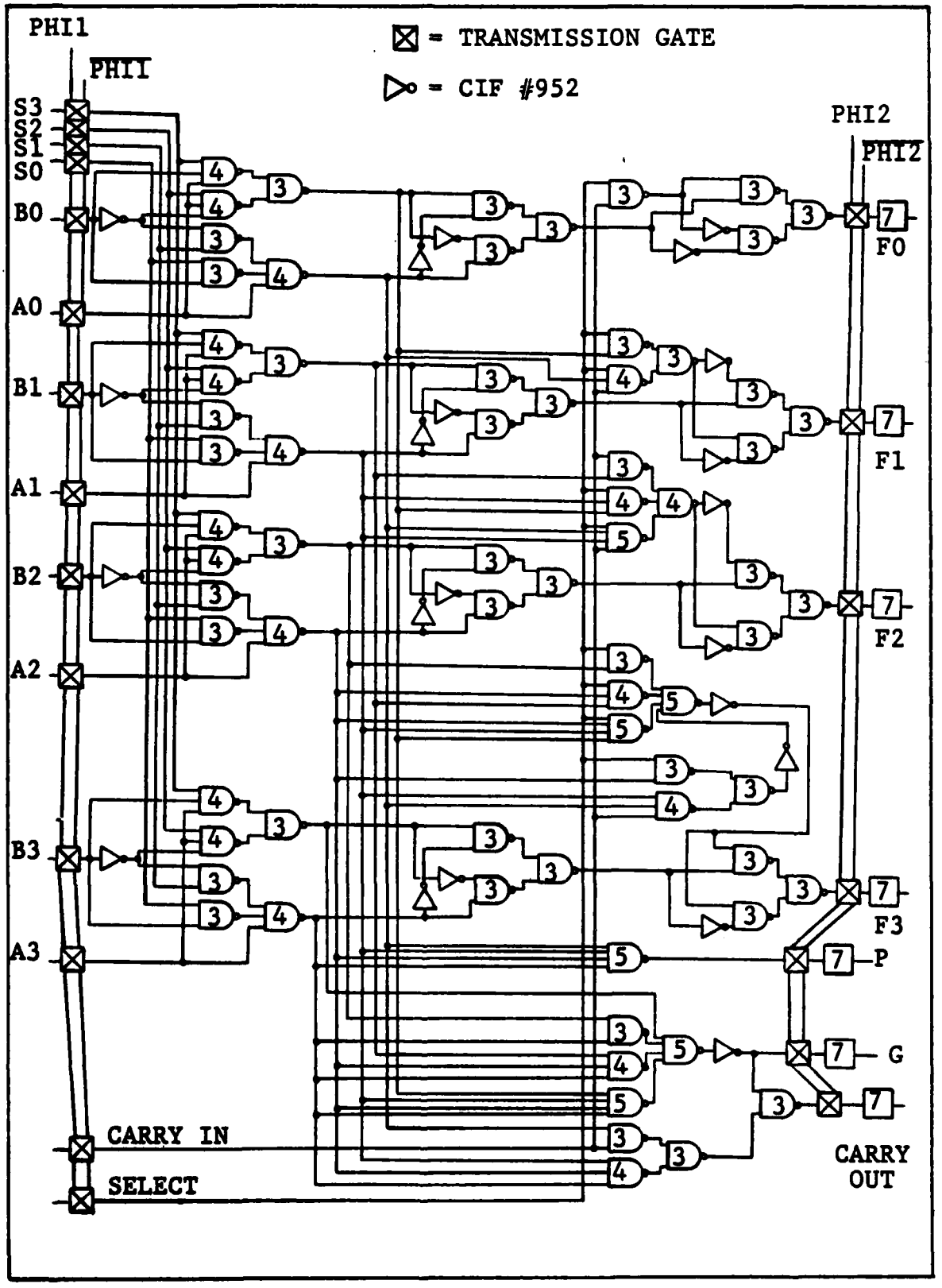


Figure V-7 4-Bit ALU Detailed Design

word lengths greater than 16 bits. This additional circuit will not be implemented as part of this thesis project.

Table V-1 ALU Arithmetic and Logic Functions [Ref 19:6]

Function Select S3	S2	S1	S0	Logic Functions M is High F	Arithmetic Operation M is Low C_n of LSB must be High F
L	L	L	L	$F = \overline{A}$	F = A minus 1
L	L	L	H	$F = \overline{A + B}$	F = A plus (A + $\overline{B}$)
L	L	H	L	$F = \overline{A} + B$	F = A plus (A + B)
L	L	H	H	F = Logical "0"	F = A times 2
L	H	L	L	$F = \overline{A + B}$	F = (A + B) minus 1
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A + $\overline{B}$)
L	H	H	L	$F = A \oplus B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} + B$	F = (A + $\overline{B}$) minus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A + B)
H	L	H	H	F = A + B	F = (A + $\overline{B}$) plus A
H	H	L	L	F = Logical "1"	F = minus 1 (two's complement)
H	H	L	H	$F = A + \overline{B}$	F = (A + $\overline{B}$) plus 0
H	H	H	L	F = A + B	F = (A + B) plus 0
H	H	H	H	F = A	F = A plus 0

The level of the select line determines whether arithmetic or logic functions will be performed by the ALU. When the select line is high, logic operations are performed. When the select line is low, arithmetic operations are performed. An additional requirement for arithmetic operations is that the least significant carry bit of each 4-bit ALU stage must be high for proper operation. The 16 possible arithmetic and logic functions are listed in Table V-1.

As stated previously, clocking will be accomplished by means of the CMOS transmission gate. All inputs, including select line and control inputs, as well as outputs will be clocked. Inputs will be clocked in on PHI 1 and all outputs will be clocked out on PHI 2.

The numbers assigned to each logic symbol represent the last digit of the standard cell CIF ID number that will be used in the actual layout. The standard cells of Appendix B are appropriately cross referrenced. Since minor variations will occur among the four bit slices, it will not be possible to iterate a single bit slice four times to arive at the final layout. A simplified bit slice will be used as a base upon which additional logic gates and connections will added as necessary. Also, additional combinational logic and connections will be added to implement the look-ahead carry feature. Due to the fact that all standard cells tessellate vertically, most Vdd and ground lines will run vertically. The use of standard cells is expected to greatly simplify layout, in terms of both time and CLL statements.

PLA Design

All PLA cells, which are used to generate the CMOS/SOS PLA, are also illustrated in Appendix B. To illustrate how a PLA is assembled using some of these cells, two sample PLAs have been layed out as shown in Figure V-8 and Figure V-9. Both layouts are based upon derivations of a PLA layout by Seitz [Ref 8], and both pass the NMOS design rule check with only implant errors (as expected). The main differences are that the PLA of Figure V-8 is highly irregular but smaller in area than the other, and they do not use an identical set of PLA cells.

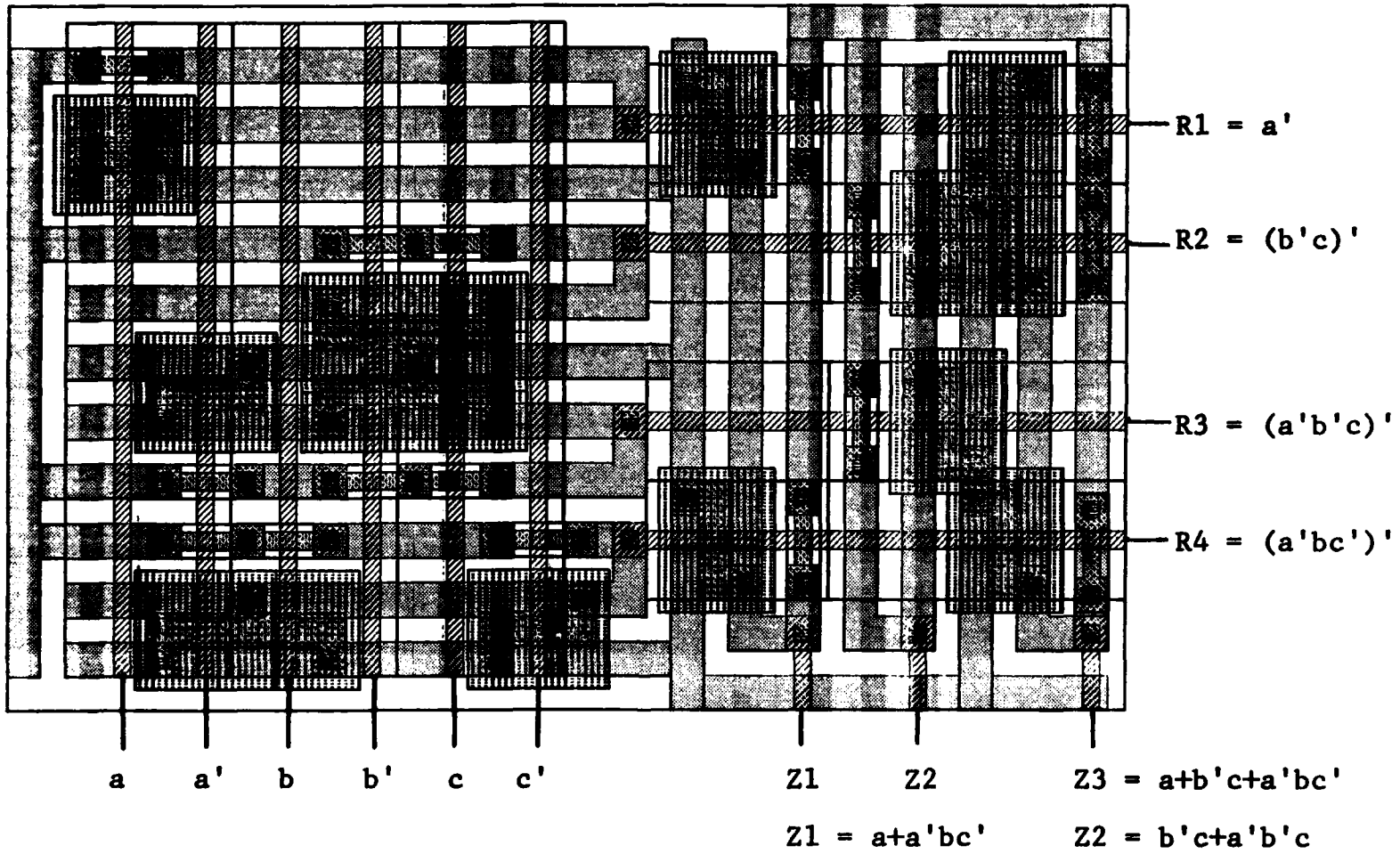


Figure V-8 Small Irregular PLA Layout

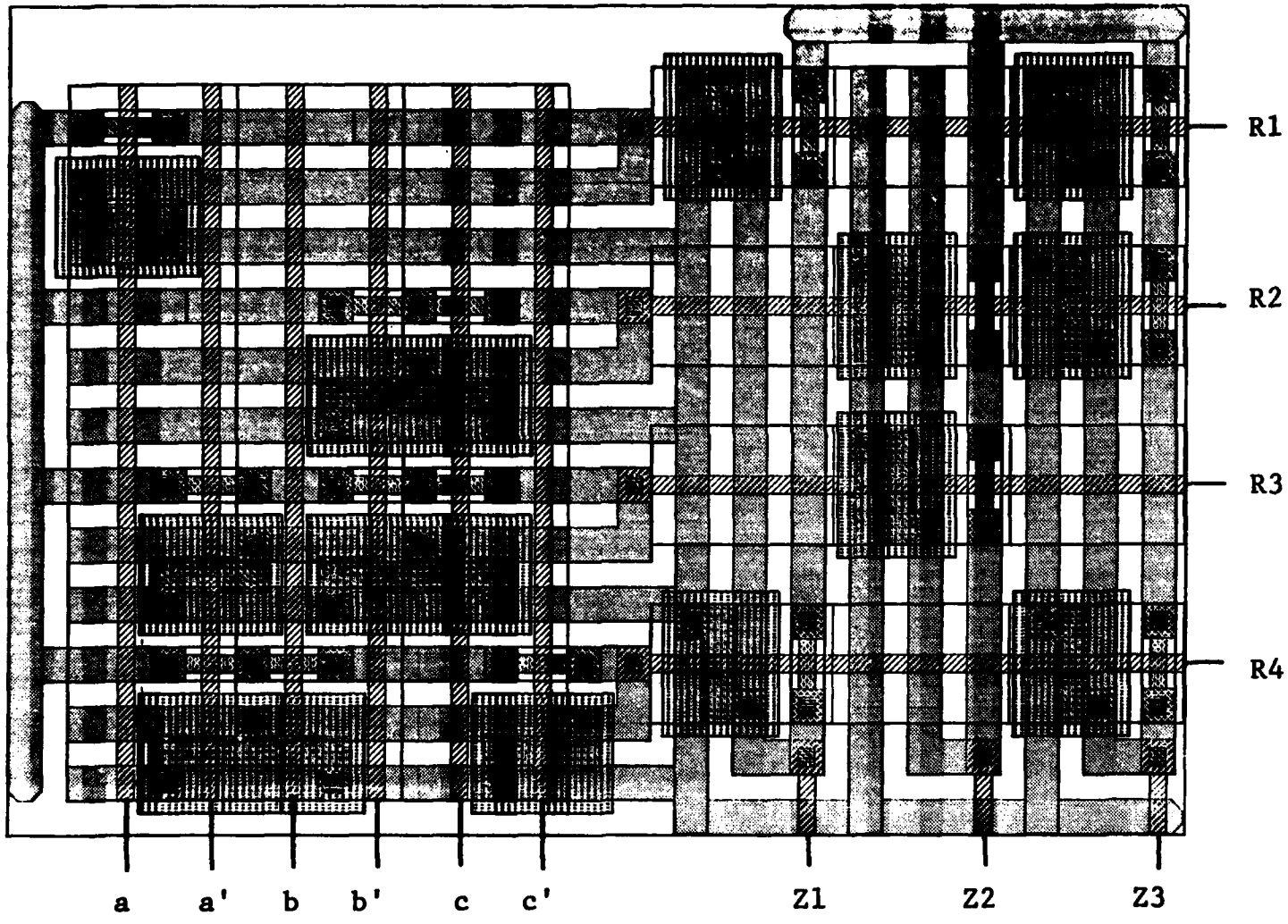


Figure V-9 Large Regular PLA Layout

Several questions had to be addressed before one of the two implementation approaches was decided upon. Circuit area was a major concern, as is evidenced by semiconductor manufacturers who continually strive to increase profits by designing circuits which have higher yields per chip. Obviously, smaller circuits help attain this goal, and they are also inherently faster. Since the PLA generator will be used mostly in the fulfillment of classroom VLSI design projects, size is probably not a great concern. But the difference in size can become significant. For example, for every odd product and output term after the first term, the larger PLA increases by seven lambda over the smaller PLA in each dimension. The only problem with the later is that its software design will be more difficult due to its irregular features. Several reasons, including time constraints, persuaded this author to attempt the more regular design of Figure V-9. Justification is based upon the following:

1. Regardless of the success of simulations, the layout of the PLA requires validation through testing of physical devices.

2. Time may not be available to complete the smaller PLA design, eliminating the possibly of fabrication and testing.

3. Completing the larger design will ensure that future AFIT VLSI design classes have a working, if not optimum, CMOS/SOS PLA generator available for experimentation.

Perhaps the design of a tool to generate the other form of the PLA, or an entirely different PLA altogether, will be

undertaken by an ambitious student of a future VLSI design class.

Operation of the larger PLA was verified using SPICE analysis (see Appendix D). In order to decrease the possibilities of error while determining circuit nodes, CIFPLOT was used with its "-X" option to produce a plot of the PLA with automatically numbered and labled nodes.

A 2x3x3 PLA was used, and all four possible input conditions were simulated. The PLA truth table and associated sum-of-product output equations are listed below.

PLA Truth Table

a	a'	b	b'	z1	z2
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	0	0

PLA Output Equations

z1 = a'b
z2 = a'b' + ab'

The CMOS/SOS PLA simulated almost exactly as predicted. For each input, all truth table values were achieved, thus verifying operation of the PLA. The reader is referred to Appendix E for a listing of all input conditions and resulting transient responses. The only potential problem obvious from the SPICE analyses is a slight asymmetry between pull-up and pull-down responses. This was apparently caused by the chance occurrence of two NMOS transistors being in series, resulting in an overall increased pull-down delay. Similar problems pertaining to NAND and NOR standard cells were discussed in Chapter V.

NMOS transistor widths may need to be increased to provide a faster pull-down transition. Making NMOS widths equal to PMOS widths (4L) should provide a more symmetrical response, without affecting PLA size. A more complete analysis is provided in Chapter VI where the CMOS/SOS PLA is compared to the Stanford NMOS PLA.

The PLA (less clocking options) consists of a total of 13 PLA cells, a few of which are discussed in this section. The basic AND and OR planes are made up of PLA cell pieces which consist of 4 lambda wide metal strips crossed at right angles by 2 lambda wide polysilicon paths. An example of a PLA cell, "CCELL", is shown in Figure V-10.

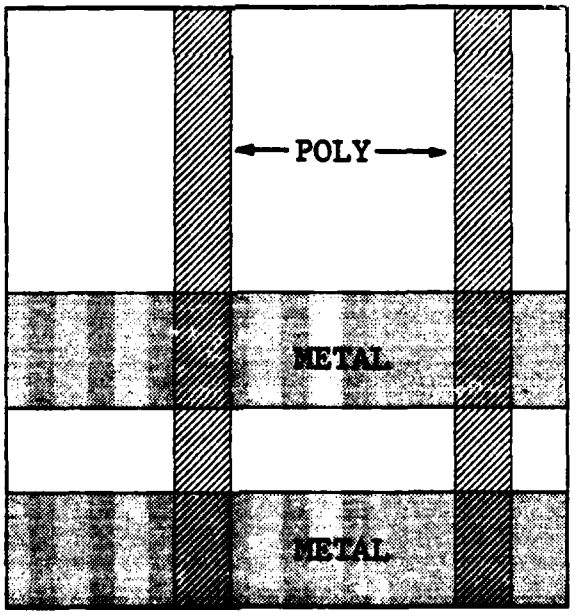
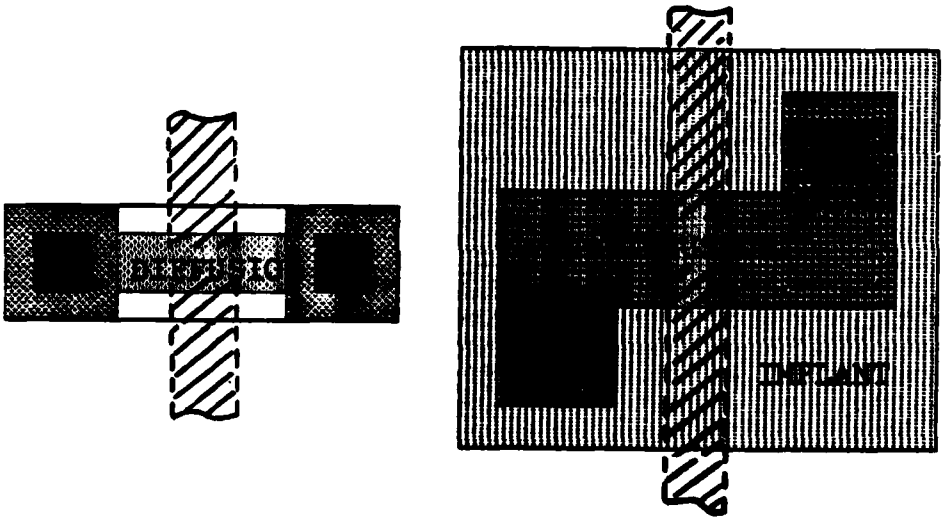


Figure V-10 Layout of CCELL

Two different PLA cells were necessary; one to compose the AND plane and another to implement the OR plane. "CCELL" is

used to construct rows and columns of the AND plane, and "CCELLR" is used to construct the OR plane. However, this latter cell does not directly connect vertically, so PLA cell space pieces (CCELLSP) are used to provide continuity of metal connections.

The NMOS and PMOS transistors are formed by crossing a polysilicon path with diffusion, or diffusion intersected with implant. The cells that form these connections are shown in Figures V-11a and b, and are called simply, "NMOS" and "PMOS". The "PMOS" piece is surrounded with implant to



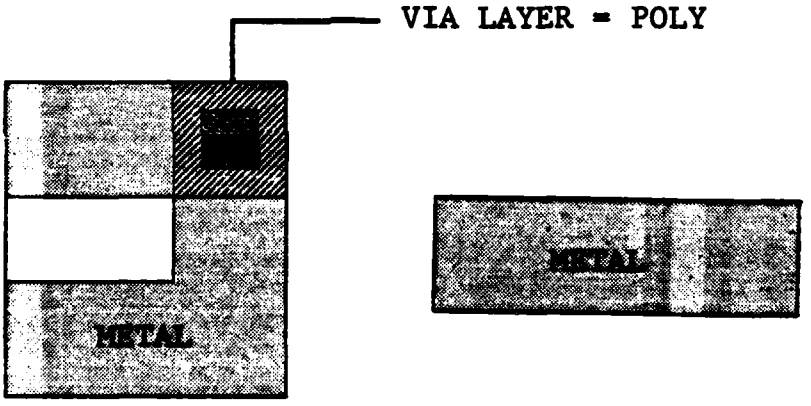
(a) NMOS PLA Cell (b) PMOS PLA Cell

Figure V-11

distinguish the PMOS transistor from the NMOS transistor during fabrication. The reader will recall the implant mask is used twice during fabrication; once to define the areas underneath the transistor gate, and a second time (in its light and dark field forms) to define doping of the source and drain areas. The PMOS cell must cross polysilicon and

connect to metal at both ends, by means of the vias, in order to form a PMOS transistor. The "NMOS" cell must cross polysilicon where there is no metal in order to form a NMOS transistor. NMOS space cells (NSPACE) are used to fill in the metal connections where NMOS transistors are absent. The dashed and cross-hatched lines of Figure V-11 represent polysilicon paths and how NMOS and PMOS cells must be oriented with respect to these paths for proper operation.

The two PLA planes are connected by means of two types of PLA connect cells. Both are shown in Figure V-12a and b and serve merely to connect the product terms to



(a) PLA Connect 1 (b) PLA Connect 2

Figure V-12 PLA Connect Cells

polysilicon paths in the OR plane and to provide continuity for the VDD buss. The PLA connect cells, rotated 90 degrees, are also used at the outputs and to provide Vdd buss connections. Other miscellaneous metal pieces are used to provide connections to the perimeter ground busses.

These ground busses are formed by continuous metal wires.

A minor amount of overlap among various cells exists throughout the PLA. The overlapping should not cause fabrication problems as it merely serves to limit the total number of PLA cells to a workable size. Some authors however, caution that repetitive overlapping of identical layers in photoresist can cause blooming of a desired shape or pattern. Apparently, some pattern generation processes cannot handle overlapping layers. Thus, repeated flashes of optical mask-generation equipment can overexpose layers and cause the blooming effect. Hon and Sequin of Xerox Parc state, however, that a CIF file should be processed to remove overlaps, and that since this process depends on the type of pattern generation used, it should be the responsibility of the fabricator, not the designer, to alleviate potential overlap problems [Ref 16].

PLA Clock In/Out Cells These cells may be considered standard cells except they are designed for horizontal tesselation. The function of the PLA clock-in cell is to provide both an inverted and noninverted clocked input to the PLA. It accomplishes this function by using derivatives of two previously described standard cells, the inverter and transmission gate.

A limitation exists with the PLA clock-in cell which will probably lower the maximum clock speed of the PLA. That is, since the input is split into two inputs and one is inverted, a delay will exist with the inverted input. In

order to layout cells that would butt directly to the PLA inputs, small gate widths had to be used resulting in an inverter delay of approximately 10 nsec. No method could be found to buffer the noninverted input to achieve a symmetrical delay.

The PLA clock-out cell is merely a transmission gate elongated and modified to directly butt to the PLA output. This cell may be horizontally tessellated with default spacing so external connections are not required. The PLA clock-in cell has five required inputs; the PLA input, Vdd and ground, and Phi 1 and not Phi 1 clock signals. The clock-out cell requires only Phi 2 and not Phi 2 as inputs, and provides the PLA sum of product terms as outputs.

Software Design

This section provides a further breakdown of certain structure chart modules presented in Chapter IV. Module 1.1, Check Input File For Errors, and module 1.4, Terminate CIF File, require few modifications, and thus, will be extracted from PLAGEN for use in the CMOS/SOS PLA generator. Module 1.2, Initiate CIF File, will be extremely similar to that written for PLAGEN. The only difference is the substitution of CMOS/SOS PLA cells in place of NMOS cells. The operation of these modules will be briefly discussed, but additional structure charts are not provided. [Ref 3]

To reaquaint the reader with the input file format to PLAGEN, it consists of a command line followed by rows

and columns of ones, dashes, and/or zeroes. The command line provides the number of inputs, number of product terms, and number of outputs and also the PLA symbol number and lambda, in that order. Error detection is not very extensive but does provide checking to insure the first line contains five arguments and the following rows and columns do not contain extraneous characters.

Initialization of the CIF file requires three activities; the calculation of lambda in hundredths of microns, writing external reference records for the CIF loader, and writing the definition of the PLA symbol. External reference records are denoted by means of what is actually the CLL "External Command", enclosed in parenthesis. These records become integral parts of any CIF file produced by CLL and are necessary for archived files. An example of an external definition of the PLA piece "NMOS" would be "(ext 1);". These definitions are required for all PLA cells including the clock-in and clock-out cells.

An example of the CIF definition of a PLA symbol is as follows:

DS 901 400 1

DS is the CIF "Define Symbol" command, "901" represents a symbol number assigned to the PLA, "400" is the CMOS/SOS lambda in hundredths of microns, and "1" is simply a scaling factor [Ref 16].

To terminate the CIF file, the CIF define finish "DF" command is written as the last line of the file. Another function included in this module, though not related the CIF file itself, is that which notifies the user of the CIF bounds. These bounds must be written in the CLL file in which the PLA is called. The bounds and size of the PLA may be calculated from the number of inputs, product terms, and outputs, and also, the presence or absence of clocking options.

Due to the significant differences between the NMOS and CMOS/SOS PLAs, module 1.3, Assemble PLA Pieces, will be completely rewritten. As noted in Chapter IV, it had three submodules, two of which require further subdivision. Module 1.3.1, Assemble PLA Planes, is broken down into subordinate modules as shown in Figure V-13. The four submodules represent functions which can, by nature, be accomplished separately and without the knowledge of actual input or output terms.

The entire PLA, less the NMOS and PMOS transistor cells, may be generated from the number of inputs, product terms, and outputs. This is accomplished by determining the x and y coordinates, and any necessary transformations, for each of the pertinent PLA cells. Coordinates are determined based on the widths and heights of each cell, given in Appendix B. For example, a PLA cell may be placed in the upper left corner of the PLA. Then, the next PLA cell in the same row would have the same y coordinate, but its x

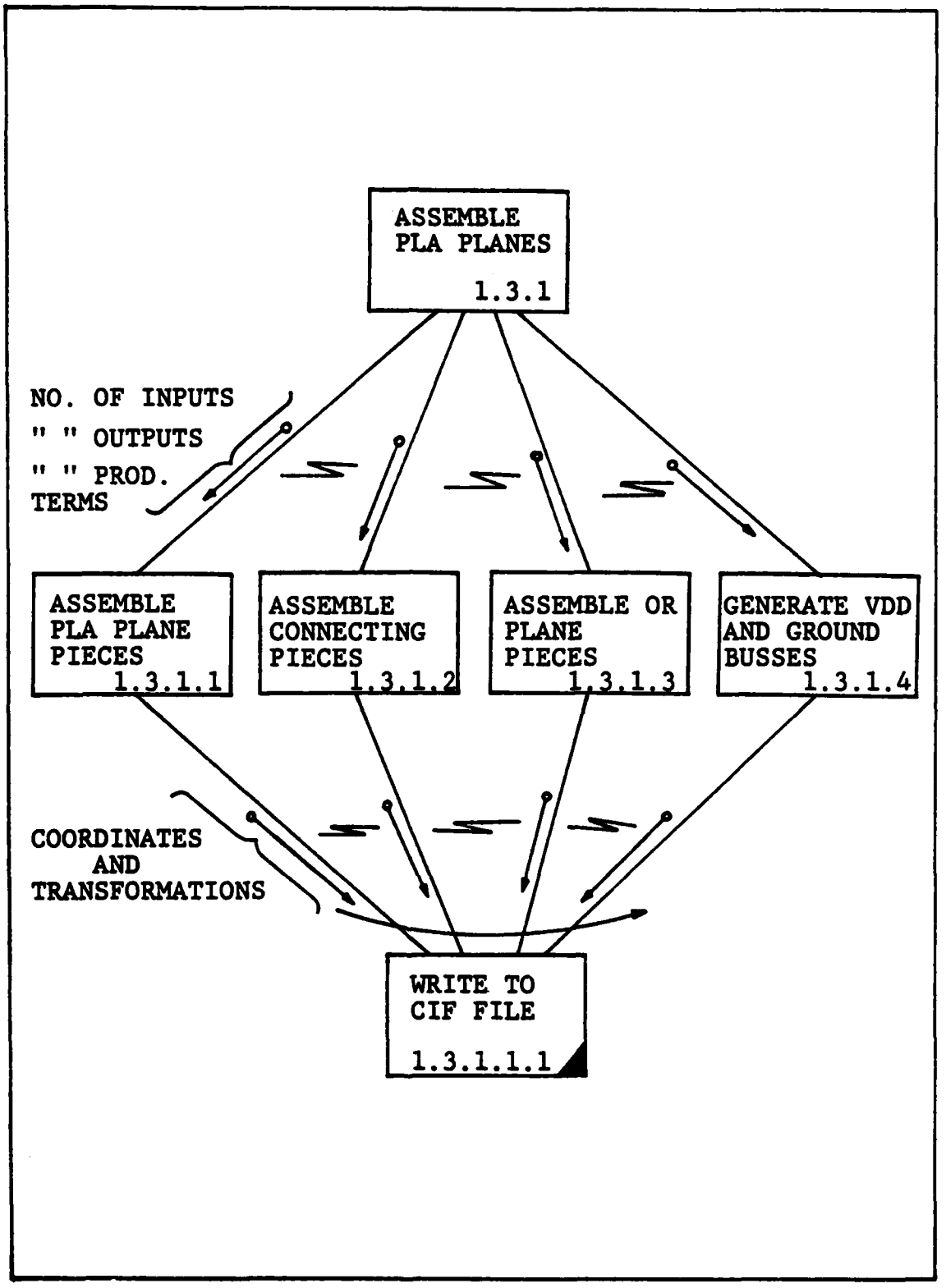


Figure V-13 Module 1.3.1 Assemble PLA Planes

coordinate would be the first x coordinate plus 20, the width of the cell. The next cell down in the same column would have the same x coordinate, but its y coordinate would be the starting y coordinate minus 21, the height of the cell. Coordinates for all PLA cells are determined in an analogous manner with a few exceptions.

In order to reduce the total number of different PLA cells, some must be rotated or mirrored in either the x or y direction. As mentioned in Chapter IV, the CIF call command "C" is used to specify transformations, rotations, and whether a cell should be mirrored. An example of the basic format for this command is as follows:

C #2 Mirrored in X Rotated to 1,1 then translated to x,y

This particular call would identify symbol number 2, the "PMOS" cell, cause it to be mirrored in the X direction, rotate it to the point 1,1 (45 degrees), and then place the origin of the cell at point X,Y [Ref 16]. Module 1.3.1.1.1, Write to CIF File, accomplishes some or all of these actions based on the quantity of information passed. This module will be required to detect the necessary transformations and write the appropriate CIF statements to the output file.

The NMOS and PMOS cells are positioned according to the value of the input and output terms. The three possibilities are a "1", "0", or a "-". Module 1.3.2, Program Inputs/Outputs, may thus be broken down into the

modules shown in Figure V-14. If the term is a 1, both

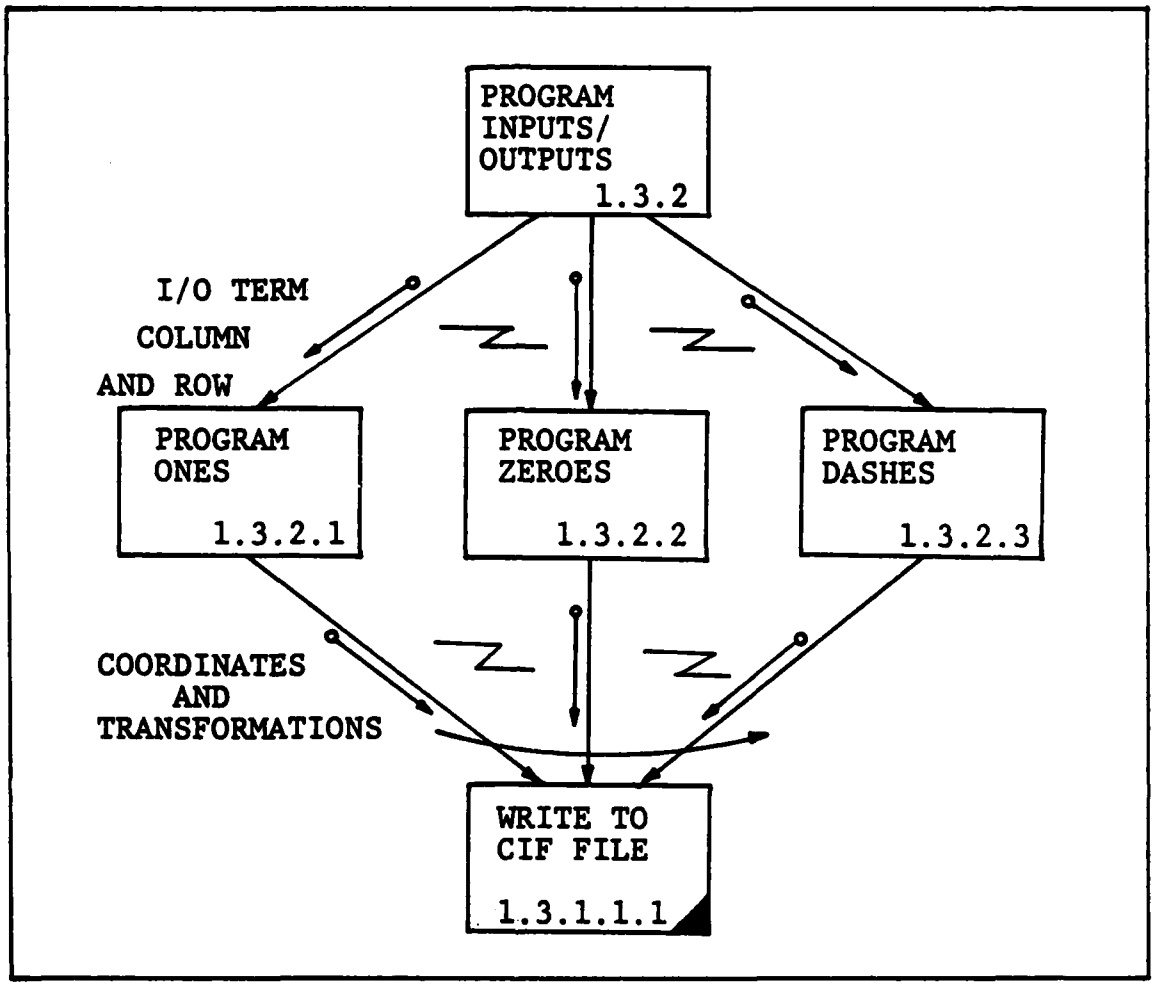


Figure V-14 Module 1.3.2 Program Inputs/Outputs

NMOS and PMOS cells are placed across the uncomplemented input polysilicon path. Conversely, if the input term is a zero, they are placed across the complemented polysilicon path. A term that is a dash indicates that no transistors are to be formed, requiring the placement of NMOS space cells.

For outputs, dashes represent ones, and require

placement of transistors. Zeroes indicate no transistors are to be programmed. In the OR plane, all three cells must be rotated 90 degrees if they are used.

A special situation arises for "0" input terms. In this case, the PMOS cell used to program the "1" product term must be mirrored in the X direction to prevent a possible short to Vdd. If the PMOS cell is not mirrored, it may overlap a PMOS cell forming a one in the column immediately to the right. An example of this may be observed in the PLA example of Figure V-8 between the inputs b' and c.

A Few Words on Implementation

The remainder of this thesis deals with the implementation of the ideas and designs set forth in this and previous chapters. The CMOS/SOS PLA generator source code, user documentation, and test results may be found in Appendix E. The final 4-bit ALU layout as well as its CLL listing are in Appendix F. The method for converting NMOS CIF formatted files to CMOS/SOS CIF formatted files is also described in Appendix F.

AD-A138 310 THE DESIGN AND LAYOUT OF A COMPLEMENTARY METAL OXIDE SEMICONDUCTOR SILICO..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. W E SOMMARS

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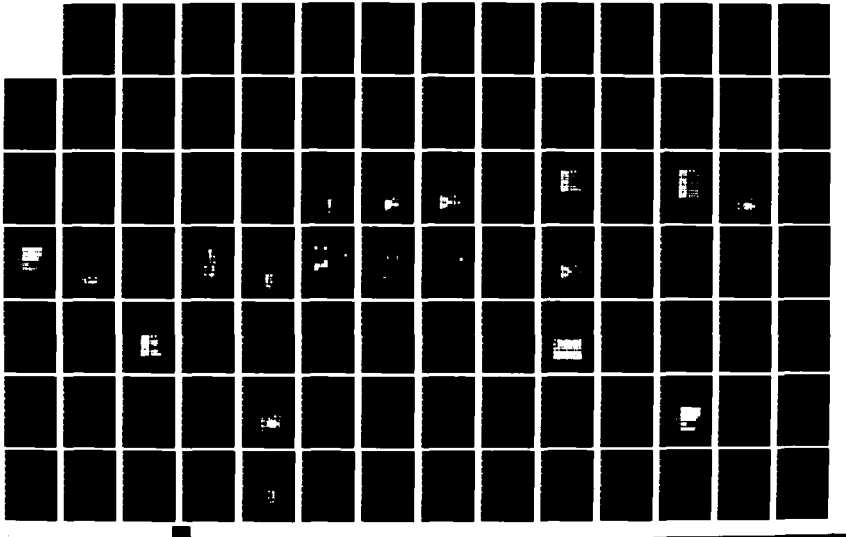

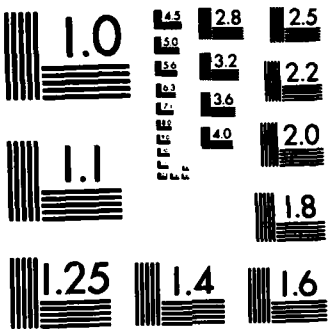

VI. Design Analysis

The design of the PLA, ALU, and standard cell library are analyzed in this chapter. In each case, the analysis attempts to provide the reader with an understanding of the functional tradeoffs, advantages, and disadvantages of the approaches undertaken throughout this thesis. Emphasis is placed upon comparisons with NMOS technology, especially the NMOS PLA and PLA generator developed by Stanford and NMOS ALU previously designed in an AFIT VLSI design course.

PLA and PLA Generator

A total of 13 PLA cells were used to generate the CMOS/SOS PLA. Two standard cells, PLA clock-in and clock-out cells, were designed specifically to simplify use of the PLA. In achieving this goal, the PLA generator "CPLAGEN" includes options for automatically placing either or both cells. In contrast, the NMOS PLA generator "PLAGEN" requires 20 different PLA cells to implement the NMOS PLA with equivalent features. Several other user transparent as well as user non-transparent features provide for interesting comparisons to the Stanford NMOS PLA.

The most obvious difference to the user is size. As was expected, the CMOS/SOS PLA is considerably larger. Table VI-1 shows the physical sizes of 10 different PLAs, ranging from very small to very large. The size is shown in

terms of width and length, both in lambda, and also in terms of the PLA area in square microns. For each case, the width and length was that computed and displayed by the programs, and the area was computed from the width, length, and definition of lambda for each technology. Lambda for CMOS/SOS is 2 microns, and lambda for NMOS is 1.25 microns. Also displayed is the percent increase in area of the CMOS/SOS PLA over the NMOS PLA.

Table VI-1 Comparison of Physical Sizes of CMOS/SOS and NMOS PLAs

	CMOS/SOS		NMOS		
PLA	Physical Size		Physical Size		% Diff
Size	WxL	Area	WxL	Area	
1x1x1	59x34	8024	68x31	3294	144
1x2x1	59x55	12980	68x31	3294	294
2x3x1	79x76	24016	84x47	6169	290
2x4x2	100x97	38800	92x47	6756	474
2x5x3	121x118	57112	100x63	9844	480
5x10x5	223x223	198916	164x95	24344	717
10x20x10	428x433	741296	284x175	77656	855
15x30x15	633x643	1628076	404x255	160969	911
20x40x20	838x853	2859256	524x343	280831	918
25x50x25	1043x1063	4434836	644x423	425644	942

Except for the smallest PLAs, the data in Table VI-1 shows a pronounced difference in PLA areas. The CMOS/SOS PLA ranges from a minimum of 144% to over 900% larger than the

NMOS PLA. The percentage increase rises sharply but begins to level off for very large PLAs.

Three reasons can be attributed to causing the large size of the CMOS/SOS PLA. The most significant factor is the difference in geometries. Minimum gate width of 1982 CMOS/SOS processes was 4 microns while the minimum for NMOS was 2.5 microns. As technological advances are made in CMOS/SOS fabrication and as both processes scale toward submicron geometries, the differences will become much less pronounced and possibly equivalent. Given no other changes, the area of the CMOS/SOS PLA would decrease by a factor of $4/[(1.25)(1.25)] = 2.56$. Another factor affecting the size of the CMOS/SOS PLA is the requirement for two transistors, NMOS and PMOS, for every transistor in the NMOS design. The extra transistor approximately doubles the size of the CMOS/SOS PLA. The third factor is due to the layout design of the PLA. Two viable layouts were presented in Chapter V, and the larger but more regular version was implemented. The larger PLA increases by 7 lambda over the smaller for each product term and output term after the first. For example, the 25x50x25 PLA could have been approximately 2.3E5 square microns smaller, not a very significant amount compared to the former two factors.

Directly related to the increased physical size of the CMOS/SOS PLA is the size of the CIF formatted file produced by the PLA generator. Although the size of the file may be considered transparent to the user, very large

PLAs may require CIF formatted files too large to be handled on some systems. A comparison of the sizes of CIF formatted files (number of lines and number of characters) produced by the CMOS/SOS PLA generator and Stanford's NMOS PLA generator are shown in Table VI-2.

Table VI-2 Comparison of Sizes of CIF Formatted Files

	CMOS/SOS		NMOS	
PLA Size	No. Lines	No. Char.	No. Lines	No. Char.
1x1x1	37	486	26	328
1x2x1	48	666	28	355
2x3x1	69	995	39	522
2x4x2	98	1489	44	551
2x5x3	137	2206	57	815
5x10x5	423	7337	135	2028
10x20x10	1553	28028	452	7158
15x30x15	3383	61785	955	15544
20x40x20	5943	109120	1680	27538
25x50x25	9223	170828	2596	42911

As was expected, the percent difference between sizes of the CMOS/SOS and NMOS CIF formatted files increases as the size of the PLAs increase, though not at the same rate as the physical size. When considering that a PLA is usually only a portion of an integrated circuit, the largest CIF file (approximately 170K) is almost prohibitively large, especially for microcomputer systems.

Because of its large physical size, problems associated with highly resistive polysilicon paths may be encountered. As an example, consider the largest PLA (25x50x25) in Table VI-1. The width of the polysilicon paths is 4 lambda. The height of the PLA was 1063 lambda, but the combined width of the top and bottom ground and Vdd busses is 11 lambda. Counting other factors, the length of the path may be rounded off to 1050 lambda. The sheet resistivity Rs of polysilicon on Sapphire is 20 ohms/square [Ref 8]. The resistance of the polysilicon path may be determined by multiplying the sheet resistivity times the aspect ratio n (n = length of wire divided by width of wire) as follows [Ref 22:116,117]:

$$
\begin{aligned}
R &= (Rs)n \\
&= (20 \text{ ohms/square})(1050/4 \text{ square}) \\
&= 5.25 \text{ Kohm}
\end{aligned}
$$

In comparison, the resistance of a metal line the same size would be be only about 13 ohms (using a sheet resistivity of 0.05 ohms/square for metal on Sapphire) [Ref 8]. The net result for very large PLAs is that highly resistive polysilicon paths could potentially reduce voltages to the point that gate charging time would be affected, or conceivably to the point that switching would not be achieved during one clock cycle.

Finally, SPICE analyses of the CMOS/SOS and NMOS PLAs are compared in terms of switching speed and power consumption for a given load. Appendix D summarizes the

procedures undertaken to simulate the PLAs. The reader is referred to that section for details. The only difference in the simulations involved the transistor models and gate geometries. A plot of the Stanford NMOS PLA was examined to determine proper gate ratios for transistors. A PLA clock-out cell was examined to determine proper ratios for the inverters on the outputs of the PLA. The reader will recall that the NMOS PLA produces inverted outputs; therefore, inverters were considered to be an integral part of the PLA even though they introduced additional delay. The CMOS/SOS PLA produces non-inverted outputs and does not require inverters.

Analysis of the SPICE transient responses indicates that the CMOS/SOS PLA exhibits a much sharper up-going transition and greater over-all symmetry between high-going and low-going transitions. During the 10nsec pulse, all transitions occured, and a steady state was achieved. The NMOS PLA however, exhibited very gradual high-going transitions and did not achieve a steady state value. In contrast, the NMOS low-going transition was very sharp, resulting in poor symmetry.

The net effect is that the CMOS/SOS PLA would probably switch faster than the NMOS PLA. The reader is cautioned to note that the pulse duration used in the SPICE analyses had a 10nsec duration which would correspond to at least a 50Mhz clock rate. At normal switching speeds (1-10Mhz), the difference would probably not be discernible.

Nevertheless, even though the results were expected, they may be somewhat difficult to understand given the larger size of the CMOS/SOS PLA. The significant difference though, is the absence of parasitic capacitances within the CMOS/SOS transistor models which resulted in faster charging and consequently, faster switching. As described in Chapter II, the Sapphire substrate has a significant effect in reducing parasitic capacitances normally found in NMOS circuits.

The SPICE analyses also verified another advantage of CMOS/SOS and CMOS in general; low power dissipation. The power consumption of the CMOS/SOS PLA was about 23.9pW while the power consumption of the NMOS PLA was about 1.83mW. Power consumption results are especially interesting since both PLAs used in the SPICE analyses required 18 transistors (counting four extra NMOS transistors for the inverters).

4-Bit ALU

Few comparisons can be made between the CMOS/SOS and NMOS ALU since the former was not tested or simulated as a complete design. Even though all individual components of the ALU were simulated using SPICE (and CIFPLOT to verify node positions on cell layouts), human error introduced during layout of the hundreds of connecting wires could not be detected.

In terms of size, the CMOS/SOS ALU is approximately equivalent to a NMOS selector circuit ALU designed by this

author during a VLSI design class at AFIT. Dimensions of the design excluding pads are 707.5 x 804 lambda, corresponding to 1415 x 1608 microns. Pads would add approximately 200 lambda to each dimension so that the final size of the ALU would be about 900 x 1000 lambda, or 1800 x 2000 microns. The NMOS ALU was 1211 x 1250 lambda, which is equivalent to 1514 x 1562 microns. It is interesting to note the 20x40x20 PLA of Table VI-1 is about the same size as the ALU with pads.

The NMOS selector logic ALU, including associated PLA and pads, was implemented with 1173 transistors. The CMOS/SOS ALU without pads required only 471 transistors. However, a total of twenty-five input and output pads, each requiring an average of about 15 transistors, need to be added to the CMOS/SOS total. Nevertheless, the total would still be considerably less than for the NMOS ALU. Apparently, the generality provided by the selector logic ALU also requires the disadvantage of more transistors, mainly in the form of a large PLA to decode the opcodes.

Standard Cell Library

The standard library cells were designed specifically to ease the design of combinational logic layouts such as the ALU. All Vdd and ground lines were vertical, and all inputs and outputs entered and exited the cells through the left and right sides respectively. That practice easily facilitated a top-down left-to-right type

layout and provided for simple layout of interconnecting wires. Vdd and ground connections, normally a designers headache, were fairly straightforward for the ALU. All individual ground busses were tied to a single large ground buss at the top of the chip, and all individual Vdd busses were tied a single large Vdd buss at the bottom of the chip. This also enabled all data busses to run vertically, thus nearly eliminating the problem of cross-overs. Though this author is undoubtedly biased toward his designs, the CMOS/SOS cells were considered easier to implement a design with than the NMOS cells.

Chapter VII. Conclusions and Recommendations

Conclusions

A CMOS/SOS PLA and PLA generator, four bit ALU, and small CMOS/SOS cell library were designed and implemented. With the exception of the PLA, all layouts were accomplished without changing existing CAD tools. The NMOS PLA generator was nearly completely rewritten because of the differences between the CMOS/SOS and NMOS PLA. Designing for readability and modularity, rather than efficiency, also required a considerable amount of restructuring.

The standard cell, PLA, and ALU layouts require more complete testing and validation. Only rudimentary circuit level and layout testing was accomplished by means of SPICE and CIFPLOT analysis respectively. Both methods lack the sophistication and thoroughness of those available for NMOS testing. Additionally, only crude design rule compliancy was tested by means of the NMOS design rule check. Though many of the NMOS design rules are the same or similar to those for CMOS/SOS, no method was available to correctly test for implant surround errors. Because of these testing deficiencies, operation of neither standard nor general cells can be guaranteed. Until actual cells are submitted for fabrication and then physically tested, even performance characteristics resulting from SPICE analysis cannot be certain. Too many variables exist to be able to completely and accurately model CMOS/SOS PMOS and NMOS devices.

An incompatibility exists with CLL and the specification of any lambda other than 2.5 lambda. The reason for the problem is unknown, though 4.0 lambda CIF formatted files can be correctly processed with CIFPLOT. The only constraint imposed upon the user is that the CIF file submitted for fabrication must be edited to incorporate 4.0 lambda geometry.

Recommendations

Validation of all CMOS/SOS designs must be accomplished. Several methods and alternatives are available: [Ref 23]

1. Submit a test chip (chips) for fabrication. Test the overall circuit and individual components by means of a logic analyzer and probe station/curve tracer respectively. Determine I-V and voltage transfer characteristics as well as switching characteristics.

2. Design an event-driven switch-level simulator such as Stanford's currently used for NMOS verification. A possible short-term alternative is to investigate the applicability of Berkeley's "sim2spice" for converting ".sim" files to those formatted in SPICE format. This would relieve the designer from manually determining SPICE nodes or from translating CIFPLOT labled nodes.

3. Write a design rule checking program or modify Stanford's NMOS design rule checker to accommodate CMOS/SOS rules. Alternatively, investigate Berkeley's hierarchial design rule checker "LYRA" for use with CMOS/SOS designs. "LYRA" can be made to handle different sets of design rules by using Berkeley's "rultec" which is used to compile a given set of design rules so they may be used with "LYRA".

Once CMOS/SOS design methods have been verified, a more complete CMOS/SOS cell library should be developed. The reader should note however, that the standard cell designs developed for this thesis represent only this authors interpretation of CMOS/SOS design. There are undoubtedly countless other design approaches that should be investigated. Additionally, input, output, VDD and ground, and clocking pads need to be developed.

The CMOS/SOS PLA generator should also be modified to produce the smallest possible PLA layout. Precharging of pull-up lines should also be incorporated into future PLA designs to provide faster switching characteristics, thus taking full advantage of CMOS/SOS speed. Many other variations of the standard PLA exist which should be investigated. Examples include the Storage/Logic Array (SLA) in which storage elements are embedded in the body of the logic array, and Path Programmable Logic (PPL) in which the AND and OR planes of the PLA are folded into one plane [Refs 24,25:1-4].

The ALU should be further analyzed to verify its design and layout. If deemed feasible, pads and final wiring should be added, and the design should be submitted for fabrication and subsequent physical testing.

Closer involvement with with other universities involved with CMOS/SOS design is also recommended. As long as the difference between information exchange for educational purposes and information regarding VHSIC and

ITAR can be maintained, no problems should arise. Additionally, certain benefits may be gained by analyzing industry developed CMOS/SOS designs. AFIT has already experimented with CMOS/SOS gate array design. Integration of both custom and gate array design into AFIT VLSI design classes is recommended.

The last area that should be investigated concerns both CMOS/SOS and NMOS technology, namely automatic cell placement and routing. The designer should not be conscerned with cell size nor the locations of connections on cells. Ideally, the designer should only need to know the Boolean function of a cell, its external node capacitances, and its fanout/switching-speed relationship. From these three cell characteristics, an appropriate cell for a specific design can be selected. Further, the actual physical placement and connection of the cell should be automatic.

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Appendix A

SPICE analyses are presented for the CMOS/SOS inverter models discussed in Chapter II. Various width-to-length ratios for the PMOS and NMOS transistors are tested in order to determine the best ratios for producing symmetrical rise and fall delays. Results indicate that the most symmetrical responses are achieved for 1.4:1 ratios, while others, such as 1:1 and 2:1 ratios, produce only slightly asymmetrical responses. The SPICE circuit model used for these analyses is shown in Figure A-1.

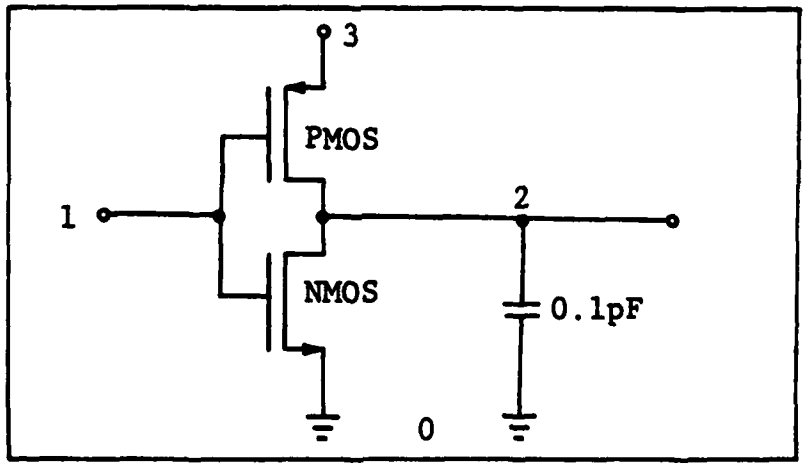


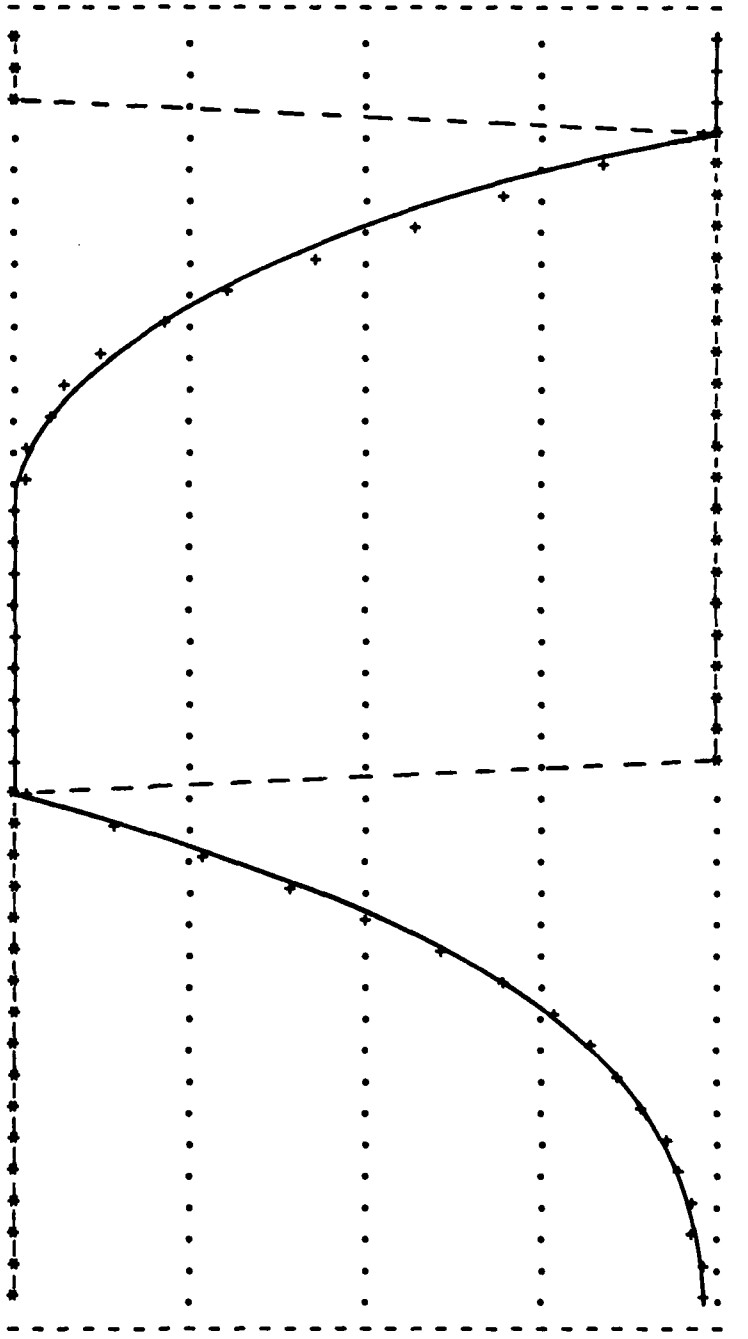
Figure A-1 SPICE CMOS/SOS Inverter Model

```
1********08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:07:21******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************



 *PARAMETERS SPECIFIED FOR MOSFET MODEL

 *VTO = ZERO-BIAS THRESHOLD VOLTAGE
 *TOX = GATE OXIDE THICKNESS
 *UO = SURFACE MOBILITY
 *NSUB = SUBSTRATE (ISLAND) DOPING
 *LD = LATERAL DIFFUSION

 *PARAMETERS CALCULATED BY SPICE

 *KP = TRANSCONDUCTANCE PARAMETER
 *GAMMA = BULK THRESHOLD PARAMETER
 *PHI = SURFACE POTENTIAL
 *CJ = ZERO-BIAS BULK JUNCTION BOTTOM CAP./M**2 OF JUNCTION PERIMETER
 *XJ = METALLURGICAL JUNCTION DEPTH

 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=2
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=2
 VDD 3 0 DC 5V
 MPD1 2 1 0 0 N L=4UM W=4UM
 MPU1 2 1 3 3 P L=4UM W=4UM
 CDBK 2 0 0.1PF
 VIN 1 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(2) (0V,5V)
 .END
1********08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:07:21******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
                N          P
OTYPE           NMOS       PMOS
OLEVEL          2.000      2.000
OVTO            1.000     -1.000
OKP          1.84d-05   9.21d-06
OGAMMA          1.979      0.685
OPHI            0.743      0.633
OCJ          5.09d-04   1.76d-04
OTOX         7.50d-08   7.50d-08
ONSUB        2.50d+16   3.00d+15
OLD          7.00d-07   7.00d-07
OUO           400.000    200.000


1********08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:07:21*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1:1)

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0**************************************************************************


  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 (  1)    0.        (  2)    5.0000    (  3)    5.0000


     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -6.933d-12

     VIN       0.   d+00

     TOTAL POWER DISSIPATION   3.47d-11  WATTS

1********08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:07:21*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1:1)

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0**************************************************************************


0
0***** MOSFETS
```

```
0            MPD1       MPU1
0MODEL     N          P
 ID        1.93d-12 -6.93d-12
 VGS          0.       -5.000
 VDS          5.000    -0.000
 VBS          0.        0.
1*******08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:07:21*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1:1)

0****     TRANSIENT ANALYSIS                TEMPERATURE =   27.000 DEG C

0*******************************************************************************
```

```
OLEGEND:

 *: V(1)
 +: V(2)
X
     TIME        V(1)

X(*+)---------- 0.    d+00      1.250d+00      2.500d+00      3.750d+00      5.000d+00
```



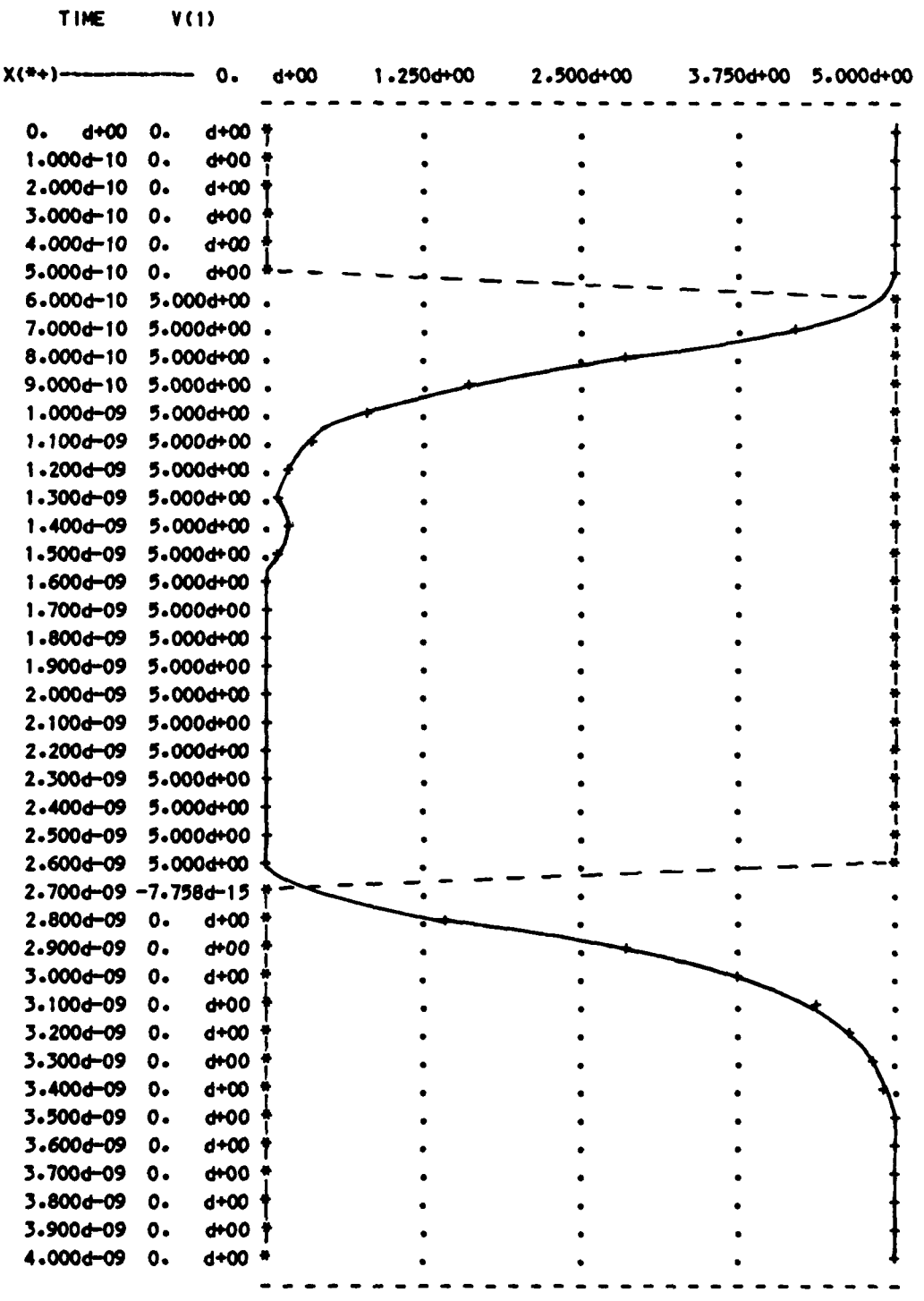
```
  0.    d+00  0.    d+00
  5.000d-10   0.    d+00
  1.000d-09   0.    d+00
  1.500d-09   5.000d+00
  2.000d-09   5.000d+00
  2.500d-09   5.000d+00
  3.000d-09   5.000d+00
  3.500d-09   5.000d+00
  4.000d-09   5.000d+00
  4.500d-09   5.000d+00
  5.000d-09   5.000d+00
  5.500d-09   5.000d+00
  6.000d-09   5.000d+00
  6.500d-09   5.000d+00
  7.000d-09   5.000d+00
  7.500d-09   5.000d+00
  8.000d-09   5.000d+00
  8.500d-09   5.000d+00
  9.000d-09   5.000d+00
  9.500d-09   5.000d+00
  1.000d-08   5.000d+00
  1.050d-08   5.000d+00
  1.100d-08   5.000d+00
  1.150d-08   5.000d+00
  1.200d-08  -8.271d-15
  1.250d-08   0.    d+00
  1.300d-08   0.    d+00
  1.350d-08   0.    d+00
  1.400d-08   0.    d+00
  1.450d-08   0.    d+00
  1.500d-08   0.    d+00
  1.550d-08   0.    d+00
  1.600d-08   0.    d+00
  1.650d-08   0.    d+00
  1.700d-08   0.    d+00
  1.750d-08   0.    d+00
  1.800d-08   0.    d+00
  1.850d-08   0.    d+00
  1.900d-08   0.    d+00
  1.950d-08   0.    d+00
  2.000d-08   0.    d+00
```

```
1*******08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:16:45*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1.4:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************



 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=2
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=2
 VDD 3 0 DC 5V
 MPD1 2 1 0 0 N L=4UM W=4UM
 MPU1 2 1 3 3 P L=4UM W=5.6UM
 CDBK 2 0 0.01PF
 VIN 1 0 PULSE (0V 5V 0.5NS 0NS 0NS 2NS)
 .TRAN 0.1NS 4.0NS
 .PLOT TRAN V(1) V(2) (0V,5V)
 .END
1*******08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:16:45*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1.4:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                 N          P
0TYPE            NMOS       PMOS
0LEVEL             2.000      2.000
0VTO               1.000     -1.000
0KP             1.84d-05   9.21d-06
0GAMMA             1.979      0.685
0PHI               0.743      0.633
0CJ             5.09d-04   1.76d-04
0TOX            7.50d-08   7.50d-08
0NSUB           2.50d+16   3.00d+15
0LD             7.00d-07   7.00d-07
0UO              400.000    200.000
```

```
1*******08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:16:45******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1.4:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************


  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 (  1)    0.        (  2)    5.0000    (  3)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT


     VDD      -6.933d-12

     VIN       0.   d+00


     TOTAL POWER DISSIPATION   3.47d-11  WATTS

1*******08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:16:45******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1.4:1)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1      MPU1
0MODEL     N         P
 ID        1.93d-12 -6.93d-12
 VGS          0.       -5.000
 VDS          5.000    -0.000
 VBS          0.        0.
1*******08/06/83 ********  SPICE 2G.1 (15OCT80)  ********16:16:45******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 1.4:1)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

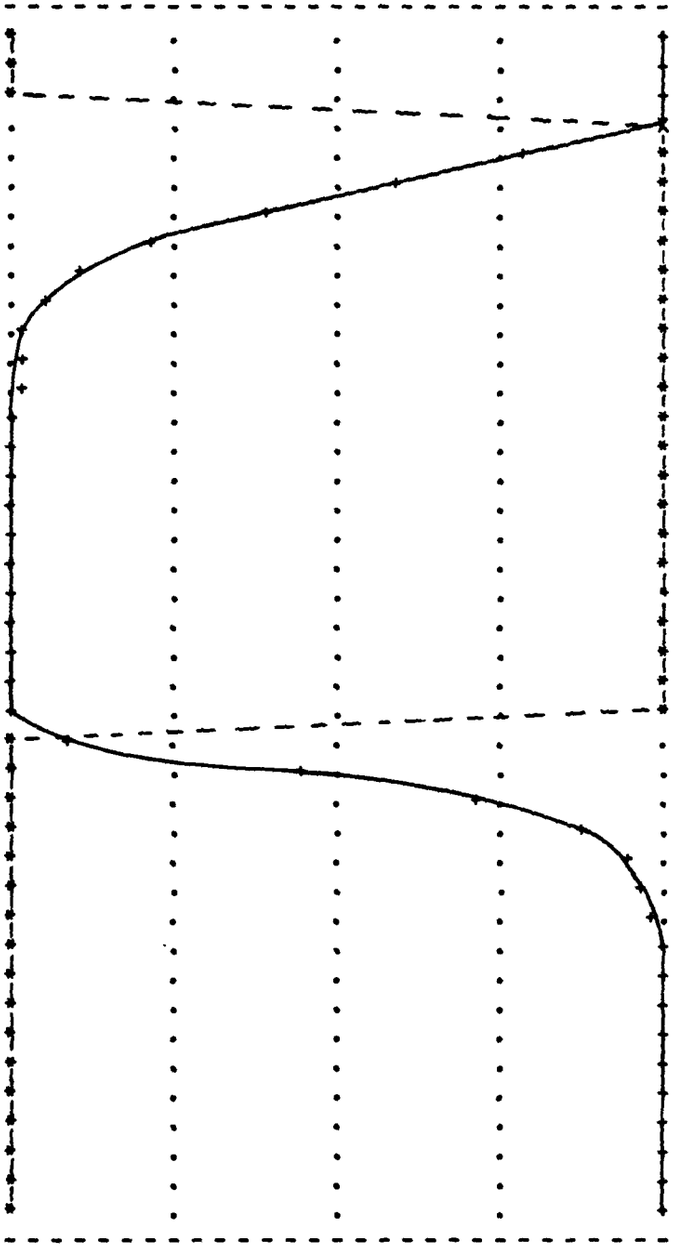
*: V(1)
+: V(2)
X



```
1********08/04/83 ********  SPICE 2G.1 (15OCT80)  ********16:28:25******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 2:1)

0****     INPUT LISTING                        TEMPERATURE =   27.000 DEG C

0*****************************************************************************



 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=2
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=2
 VDD 3 0 DC 5V
 MPD1 2 1 0 0 N L=4UM W=6UM
 MPU1 2 1 3 3 P L=4UM W=12UM
 CDBK 2 0 0.1PF
 VIN 1 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20.0NS
 .PLOT TRAN V(1) V(2) (0V,5V)
 .END
1********08/04/83 ********  SPICE 2G.1 (15OCT80)  ********16:28:25******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 2:1)

0****     MOSFET MODEL PARAMETERS              TEMPERATURE =   27.000 DEG C

0*****************************************************************************


                 N          P
0TYPE          NMOS       PMOS
0LEVEL          2.000      2.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000
```

```
1*******08/04/83 ********  SPICE 2G.1 (15OCT80)  ********16:28:25*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 2:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0**********************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 (  1)    0.        (  2)    5.0000    (  3)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -6.933d-12

     VIN       0.   d+00

     TOTAL POWER DISSIPATION   3.47d-11  WATTS

1*******08/04/83 ********  SPICE 2G.1 (15OCT80)  ********16:28:25*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 2:1)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0**********************************************************************


0
0**** MOSFETS


0             MPD1       MPU1
OMODEL      N          P
 ID         1.93d-12 -6.93d-12
 VGS           0.       -5.000
 VDS           5.000    -0.000
 VBS           0.        0.
1*******08/04/83 ********  SPICE 2G.1 (15OCT80)  ********16:28:25*****

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 2:1)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0**********************************************************************
```

```
OLEGEND:

 *: V(1)
 +: V(2)
X
     TIME        V(1)

X(*+)————————— 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
 0.   d+00  0.   d+00
 5.000d-10  0.   d+00
 1.000d-09  0.   d+00
 1.500d-09  5.000d+00
 2.000d-09  5.000d+00
 2.500d-09  5.000d+00
 3.000d-09  5.000d+00
 3.500d-09  5.000d+00
 4.000d-09  5.000d+00
 4.500d-09  5.000d+00
 5.000d-09  5.000d+00
 5.500d-09  5.000d+00
 6.000d-09  5.000d+00
 6.500d-09  5.000d+00
 7.000d-09  5.000d+00
 7.500d-09  5.000d+00
 8.000d-09  5.000d+00
 8.500d-09  5.000d+00
 9.000d-09  5.000d+00
 9.500d-09  5.000d+00
 1.000d-08  5.000d+00
 1.050d-08  5.000d+00
 1.100d-08  5.000d+00
 1.150d-08  5.000d+00
 1.200d-08 -8.257d-15
 1.250d-08  0.   d+00
 1.300d-08  0.   d+00
 1.350d-08  0.   d+00
 1.400d-08  0.   d+00
 1.450d-08  0.   d+00
 1.500d-08  0.   d+00
 1.550d-08  0.   d+00
 1.600d-08  0.   d+00
 1.650d-08  0.   d+00
 1.700d-08  0.   d+00
 1.750d-08  0.   d+00
 1.800d-08  0.   d+00
 1.850d-08  0.   d+00
 1.900d-08  0.   d+00
 1.950d-08  0.   d+00
 2.000d-08  0.   d+00
```

```
1********06/06/83 ********  SPICE 2G.1 (15OCT80)  ********12:00:16******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 3:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************



 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=2
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=2
 VDD 3 0 DC 5V
 MPD1 2 1 0 0 N L=4UM W=4UM
 MPU1 2 1 3 3 P L=4UM W=12UM
 CDBK 2 0 0.1PF
 VIN 1 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20.0NS
 .PLOT TRAN V(1) V(2) (0V,5V)
 .END
1********06/06/83 ********  SPICE 2G.1 (15OCT80)  ********12:00:16******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 3:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                N          P
0TYPE           NMOS       PMOS
0LEVEL            2.000      2.000
0VTO              1.000     -1.000
0KP           1.84d-05   9.21d-06
0GAMMA            1.979      0.685
0PHI              0.743      0.633
0CJ           5.09d-04   1.76d-04
0TOX          7.50d-08   7.50d-08
0NSUB         2.50d+16   3.00d+15
0LD           7.00d-07   7.00d-07
0UO             400.000    200.000
```

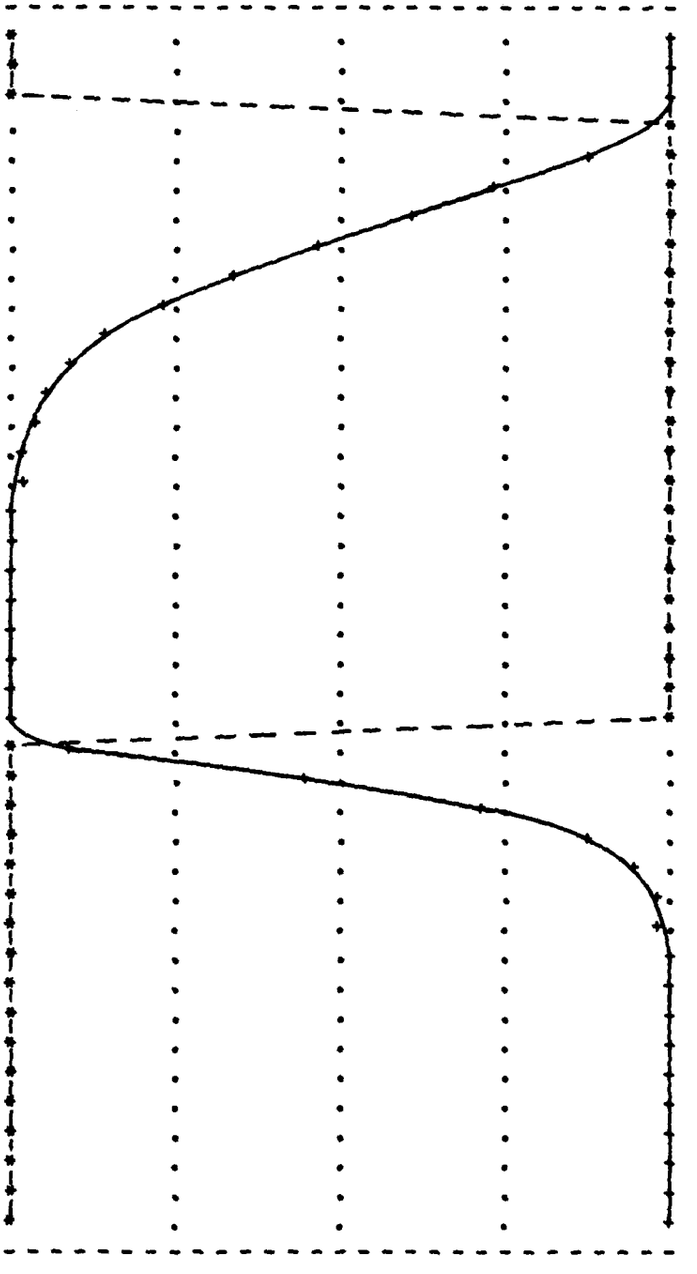
```
1*******06/06/83 ********  SPICE 2G.1 (15OCT80)  ********12:00:16******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 3:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************


  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 ( 1)    0.        ( 2)    5.0000    ( 3)    5.0000


     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT


     VDD      -6.933d-12

     VIN       0.   d+00


     TOTAL POWER DISSIPATION   3.47d-11  WATTS
1*******06/06/83 ********  SPICE 2G.1 (15OCT80)  ********12:00:16******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 3:1)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1      MPU1
0MODEL     N         P
 ID        1.93d-12 -6.93d-12
 VGS          0.       -5.000
 VDS          5.000    -0.000
 VBS          0.        0.
1*******06/06/83 ********  SPICE 2G.1 (15OCT80)  ********12:00:16******

0       CMOS/SOS INVERTER TRANSIENT ANALYSIS (W/L = 3:1)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

*: V(1)
+: V(2)
X

TIME	V(1)
0. d+00	0. d+00
5.000d-10	0. d+00
1.000d-09	0. d+00
1.500d-09	5.000d+00
2.000d-09	5.000d+00
2.500d-09	5.000d+00
3.000d-09	5.000d+00
3.500d-09	5.000d+00
4.000d-09	5.000d+00
4.500d-09	5.000d+00
5.000d-09	5.000d+00
5.500d-09	5.000d+00
6.000d-09	5.000d+00
6.500d-09	5.000d+00
7.000d-09	5.000d+00
7.500d-09	5.000d+00
8.000d-09	5.000d+00
8.500d-09	5.000d+00
9.000d-09	5.000d+00
9.500d-09	5.000d+00
1.000d-08	5.000d+00
1.050d-08	5.000d+00
1.100d-08	5.000d+00
1.150d-08	5.000d+00
1.200d-08	-8.271d-15
1.250d-08	0. d+00
1.300d-08	0. d+00
1.350d-08	0. d+00
1.400d-08	0. d+00
1.450d-08	0. d+00
1.500d-08	0. d+00
1.550d-08	0. d+00
1.600d-08	0. d+00
1.650d-08	0. d+00
1.700d-08	0. d+00
1.750d-08	0. d+00
1.800d-08	0. d+00
1.850d-08	0. d+00
1.900d-08	0. d+00
1.950d-08	0. d+00
2.000d-08	0. d+00

X(*+)———————— 0. d+00 1.250d+00 2.500d+00 3.750d+00 5.000d+00



Appendix B

The documentation is presented for each standard cell and PLA cell as set forth by the requirements of Chapter III. The documentation should be self explanatory; however, if ambiguities are discovered, they may be resolved by referring back to the appropriate section in Chapter V. Each cell was plotted using CIFPLOT, and has inputs, outputs, and other connections labled to aid potential users. The same scale was used to plot all standard cells, with the exception of the double buffered output cell, in order to show the spacial relationships between the different cells. Due to the large size of the double buffered output, a smaller scale was used so it would fit on one page. All PLA cells also use an identical scale. All power consumption was determined with a 0.1 pF load, though actual power consumption will vary with different loads and switching speeds.

An attempt was made to verify design rule correctness using the NMOS design rule checker. All standard cells showed no errors except for implant surround errors. This was expected because the implant layer for CMOS/SOS corresponds to an entirely different fabrication process than that for NMOS.

These standard cells use CIF numbers 951 through 961. Hence, the numbers should not be assigned to other CMOS/SOS cells or to any PLA used in a CMOS/SOS design.

Standard Cell: INVSLOW CIF ID: 951

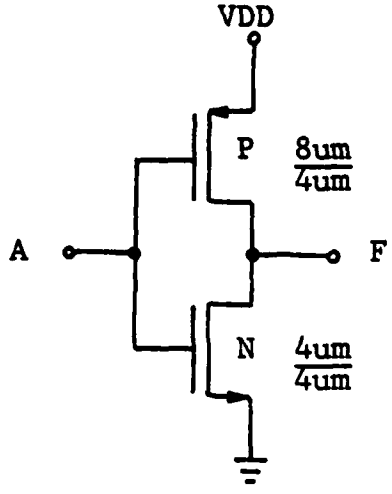
Description: Slow Inverter (W/L Ratio = 8/4:4/4)

Logic Symbol

Truth Table

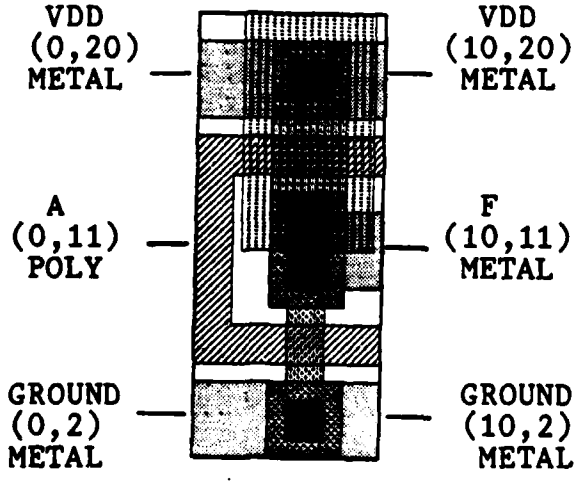
A	F
0	1
1	0

Schematic



Size: Width = 10L Length = 23.5L
Tessellation: None
Approximate Power Consumption: 34.7 pW

CIFPLOT



Standard Cell: INVFAST CIF ID: 952

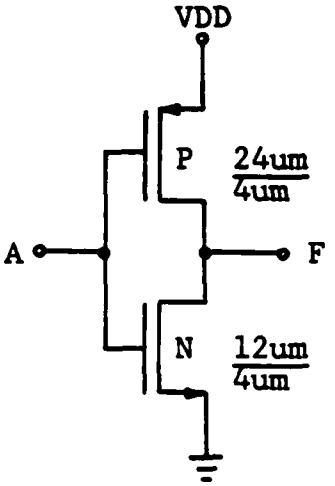
Description: Fast Inverter (W/L ratio = 8/4:12/4)

Logic Symbol

Truth Table

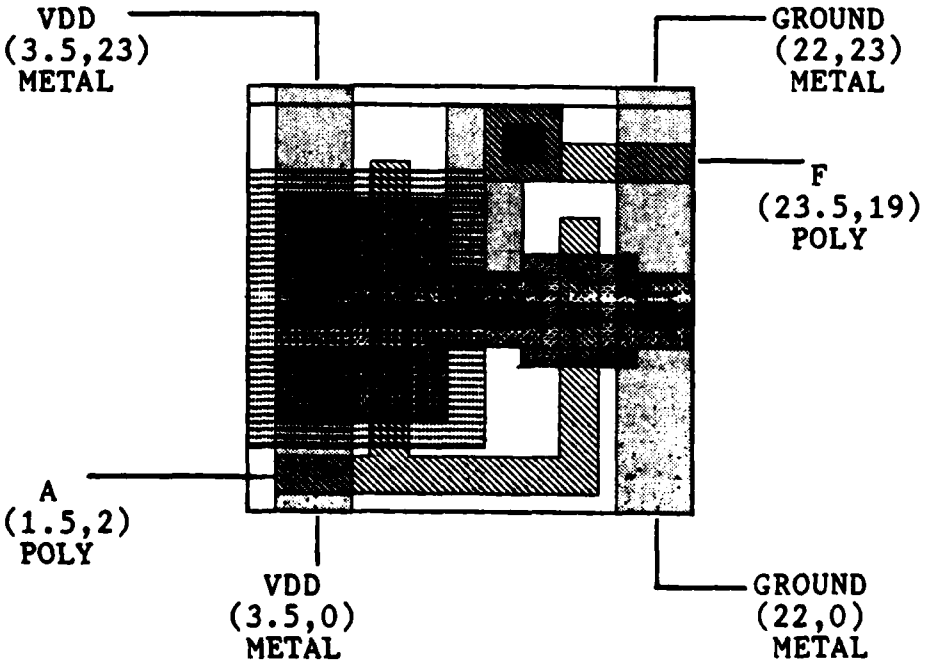
A	F
0	1
1	0

Schematic



Size: Width = 23L Length = 23.5L
Tessellation: Vertical, metal, 4L wide, 18L separation
Approximate Power Consumption: 34.7 pW

CIFPLOT



Standard Cell: NAND2 CIF ID: 953

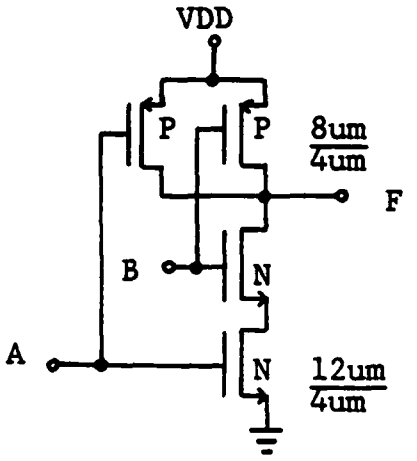
Description: Two input NAND gate

Logic Symbol

Truth Table

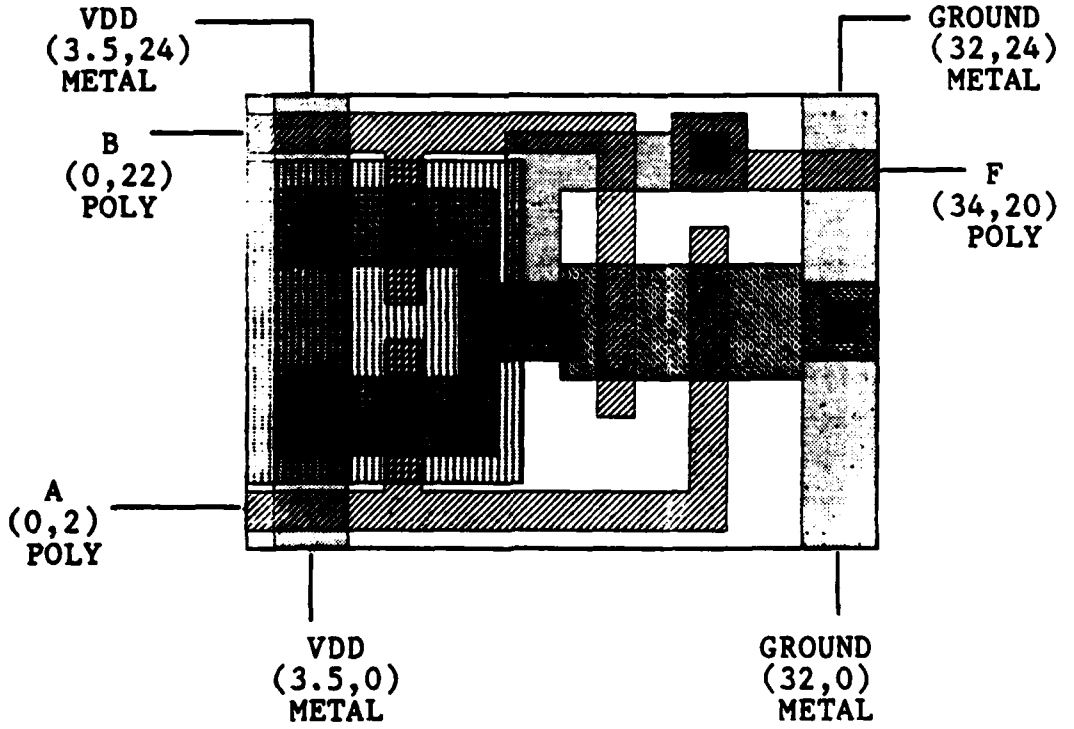
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Schematic



Size: Width = 34L Length = 24L
Tessellation: Vertical, metal, 4L wide, 28.5L separation
Aproximate Power Consumption: 173 pW

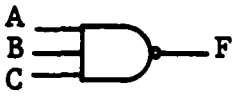
CIFPLOT



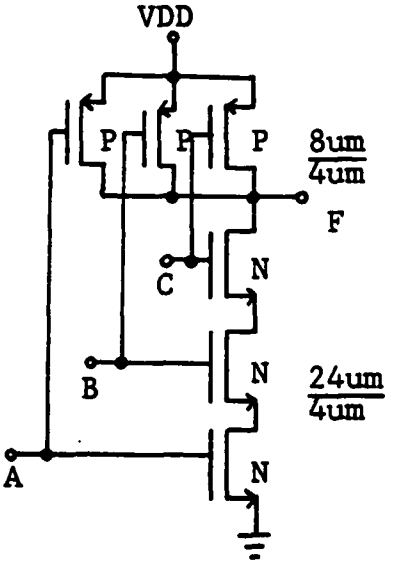
Standard Cell: NAND3 CIF ID: 954

Description: Three input NAND gate

Logic Symbol



Schematic



Truth Table

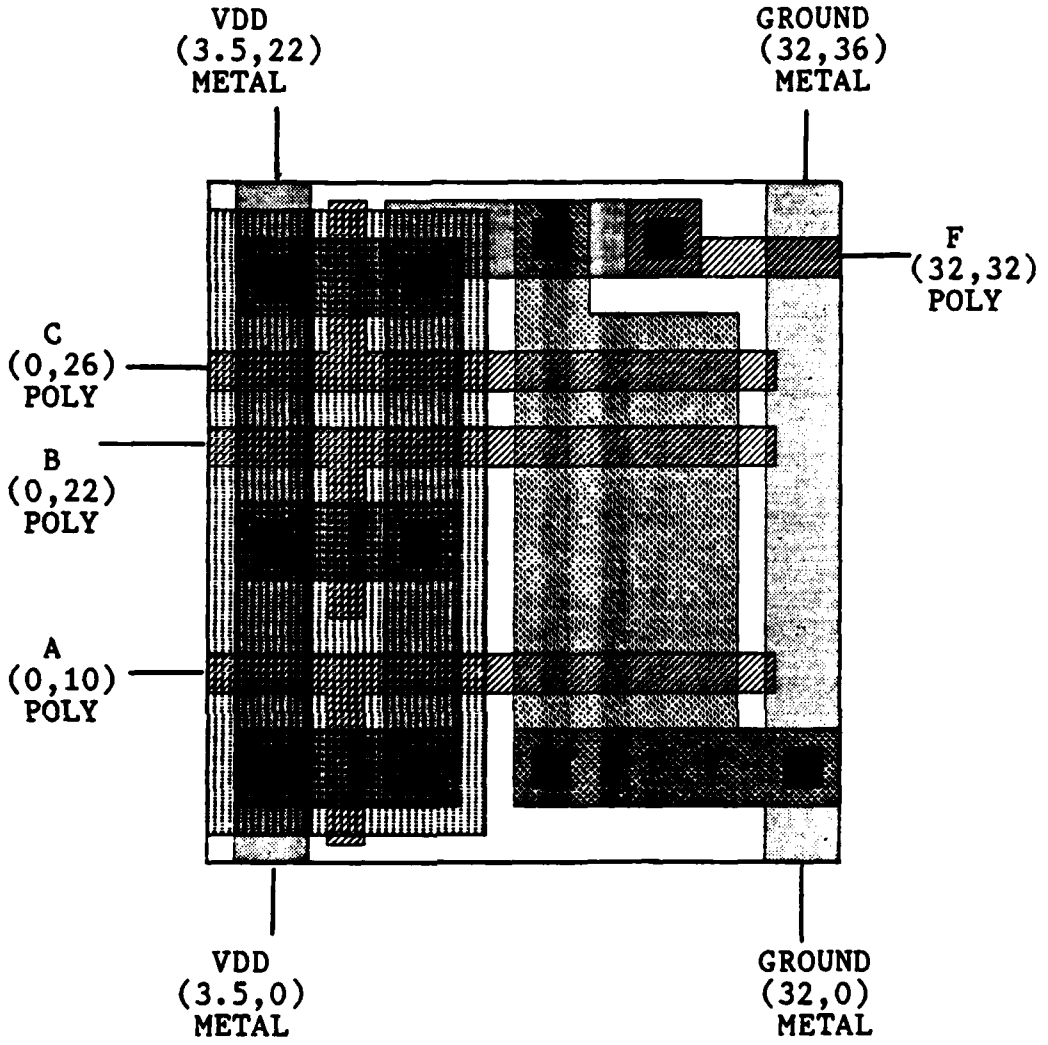
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Size: Width = 34L Length = 36L
Tesselation: Vertical, metal, 4L wide, 28.5L separation
Approximate Power Consumption: 347 pW

CIFPLOT

(SEE NEXT PAGE)

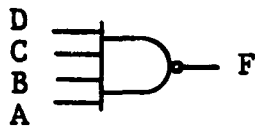
Three Input NAND (NAND3)



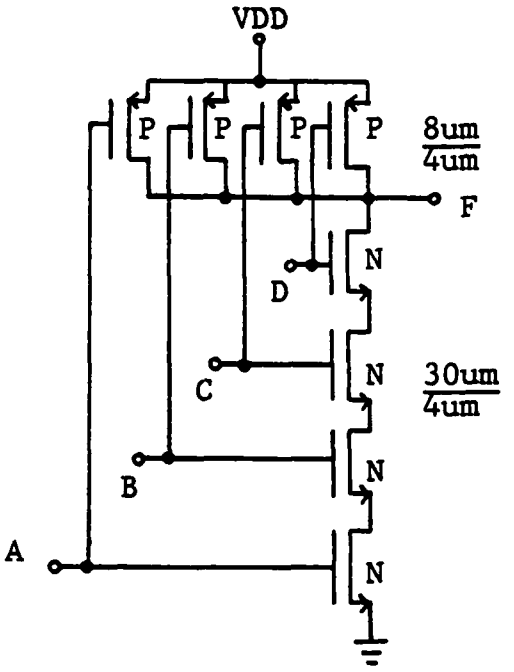
Standard Cell: NAND4 CIF ID: 955

Description: Four input NAND gate

Logic Symbol



Schematic



Truth Table

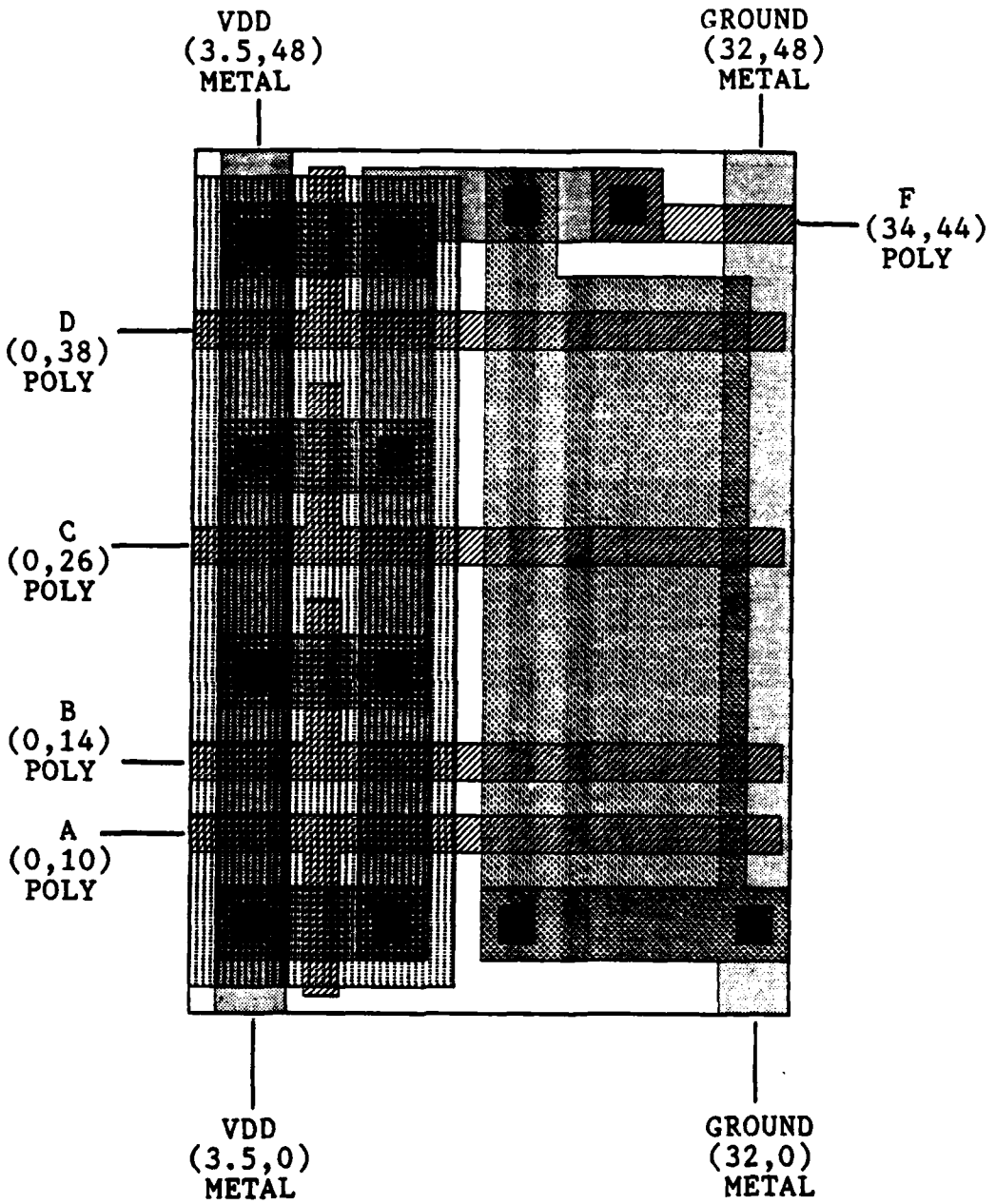
A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Size: Width = 34L Length = 48L
Tessellation: Vertical, metal, 4L wide, 28.5L separation
Approximate Power Consumption: 590 pW

Cll or Cifplot

(SEE NEXT PAGE)

Four Input NAND (NAND4)



Standard Cell: NOR CIF ID: 956

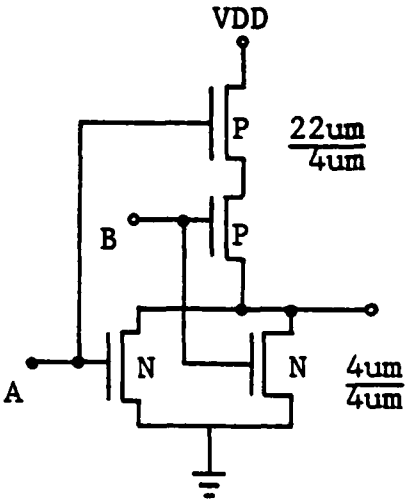
Description: Two input NOR gate

Logic Symbol

Truth Table

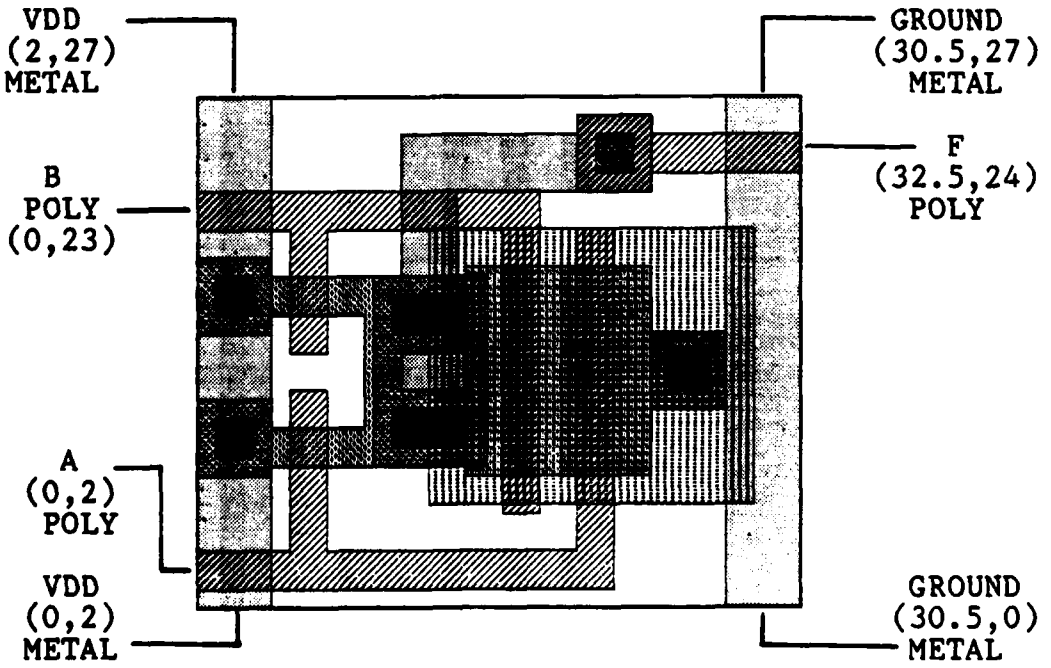
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Schematic



Size: Width = 32.5L Length = 27L
Tessellation: Vertical, metal, 4L wide, 28.5L separation
Approximate Power Consumption: 69.3 pW

Cifplot

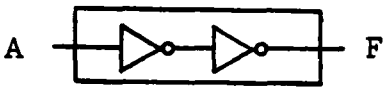


Standard Cell: DBUF CIF ID: 957

Description: Double buffered output -- used on outputs of CMOS/SOS circuits to improve voltage transfer characteristics and load driving capability.

Logic Symbol

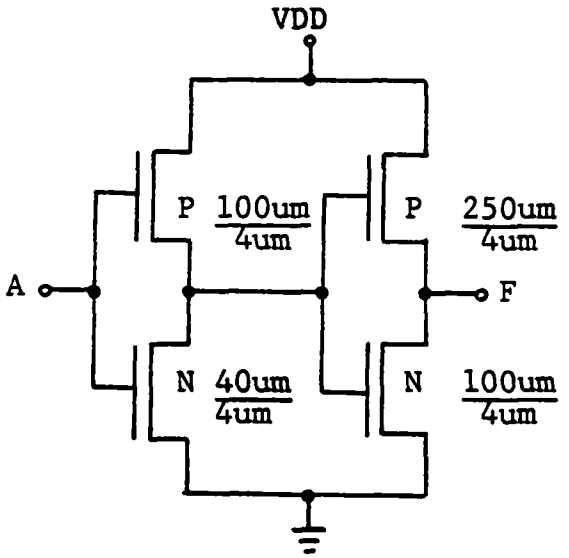
OR



Truth Table

A	F
0	0
1	1

Schematic

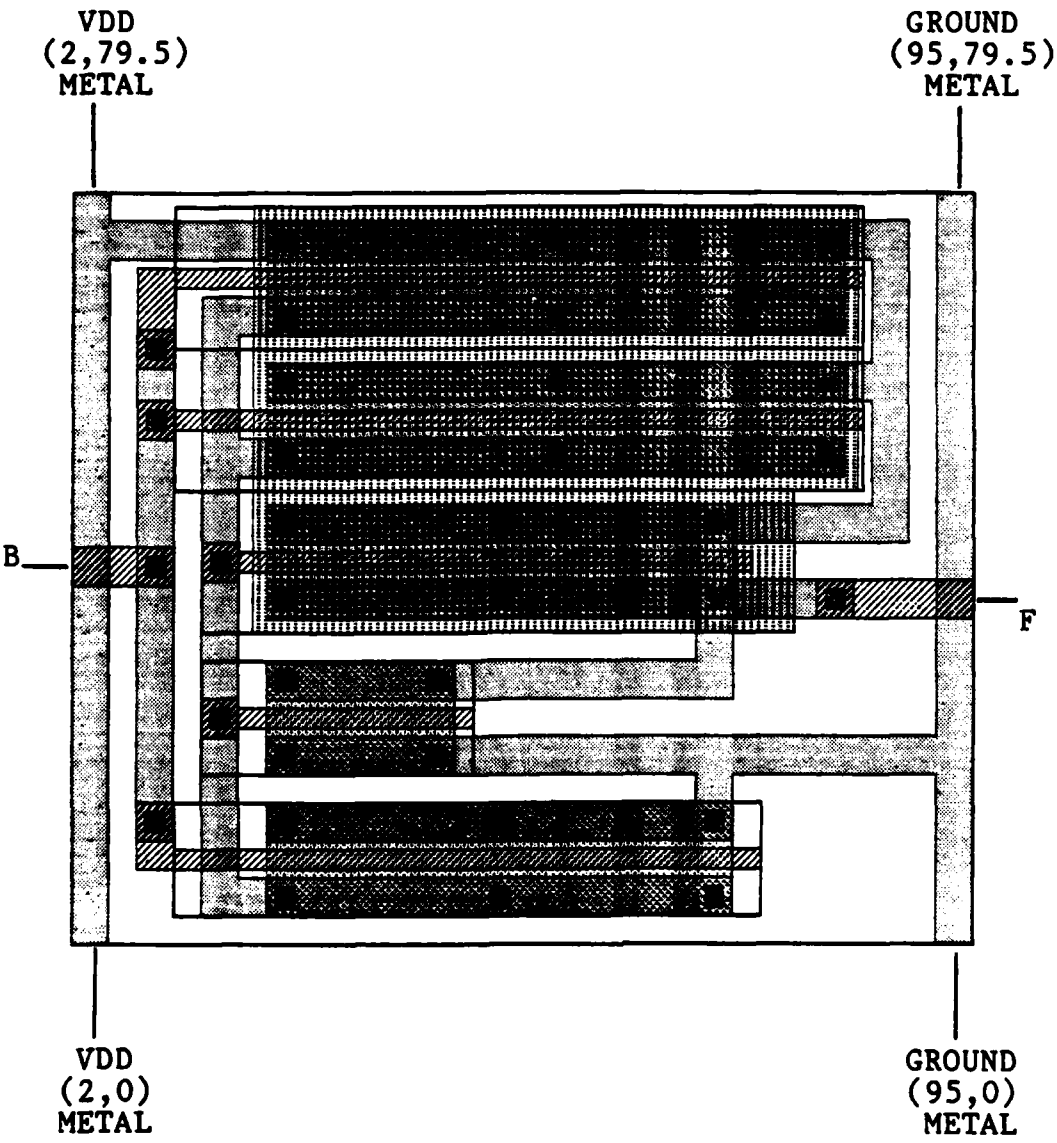


Size: Width = 97.5L Length = 79.5L
Tesselation: Vertical, metal, 4L wide, 93.5L Separation
Approximate Power Consumption: 69.3pW

CIFPLOT

(SEE NEXT PAGE)

Double Buffered Output (DBUF)

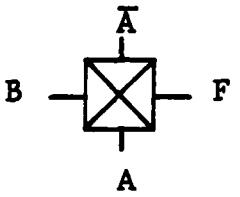


B COORDINATES: (0,40) LAYER: POLY
F COORDINATES: (97,36.5) LAYER: POLY

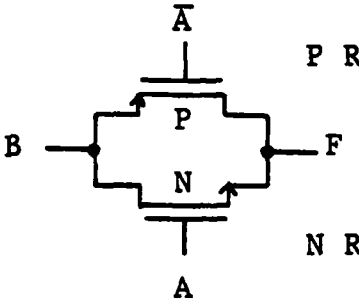
Standard Cell: TXGATE CIF ID: 958

Description: Transmission gate -- used to clock CMOS circuits. Requires an inverted and noninverted phase of a clock signal (Phi1 or Phi2). Example: Phi1 is applied to NMOS gate, and not Phi1 is applied to the PMOS gate. Passes signal bidirectionally when Phi1 is high.

Logic Symbol



Schematic



P RATIO = $\frac{8um}{4um}$

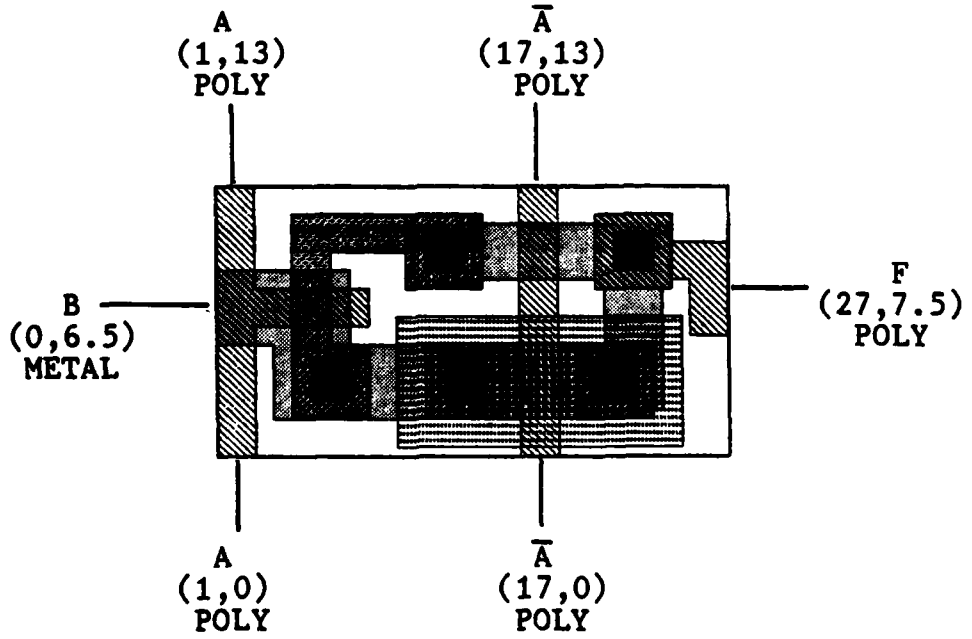
N RATIO = $\frac{4um}{4um}$

Truth Table

A	$\overline{A}$	B	F
0	1	0	X
1	0	0	0
0	1	1	X
1	0	1	1

Size: Width = 27L Length = 13L
Tesselation: Vertical, poly, 2L wide, separation = 18L
Power Dissipation: 52 pW

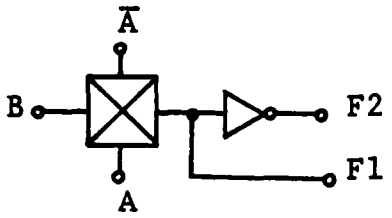
Cifplot



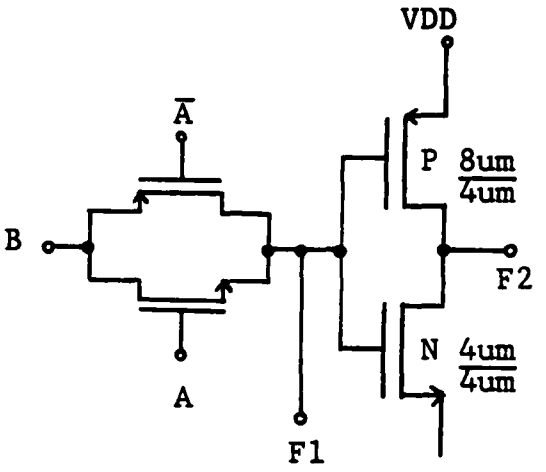
Standard Cell: PlaClkIn CIF ID: 959

Description: Pla clock in -- provides clocked inverted and noninverted inputs to Pla. Butts directly to bottom of Pla and tesselates horizontally with no overlap.

Logic Symbol



Schematic



Truth Table

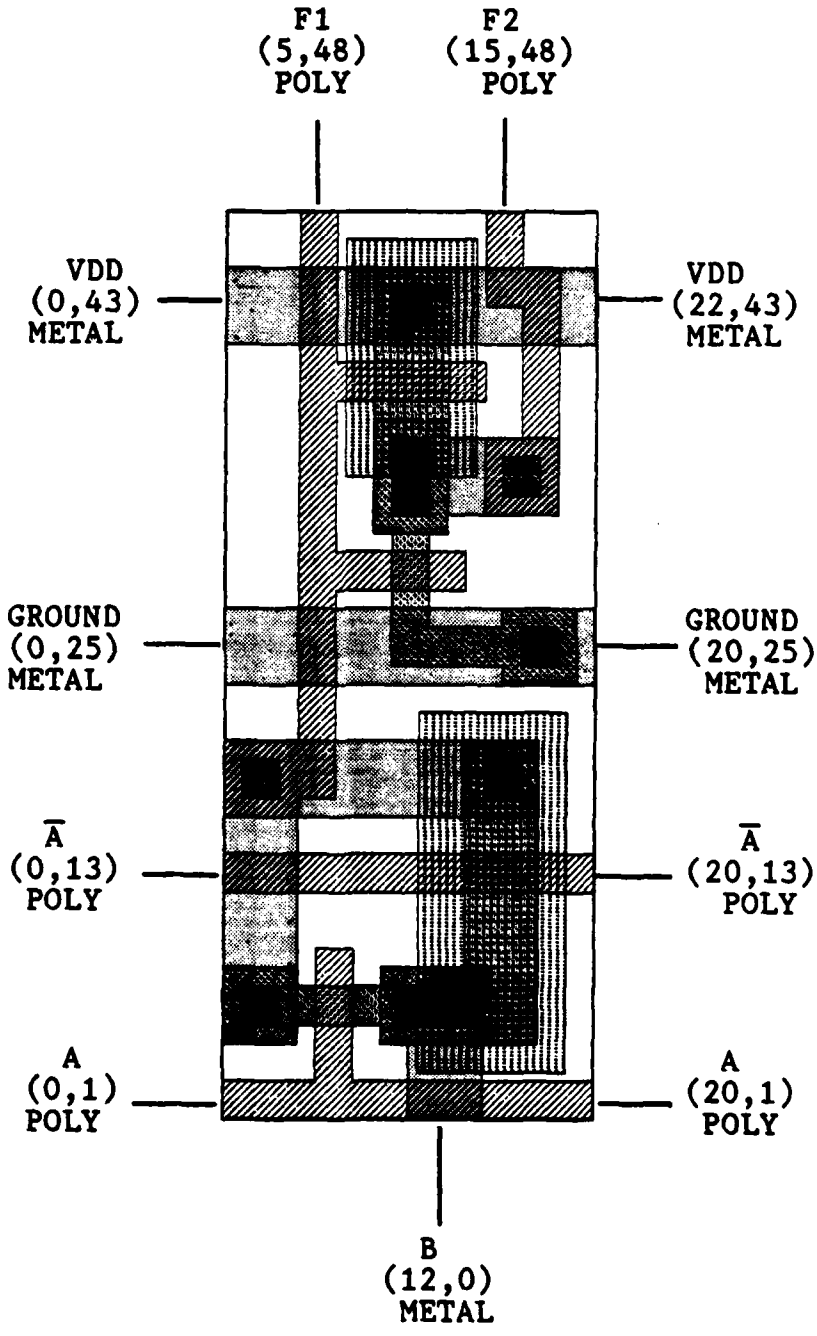
A	A	$\overline{B}$	F1	F2
0	1	0	X	X
1	0	0	0	1
0	1	1	X	X
1	0	1	1	0

Size: Width = 20L Length = 48L
Tesselation: Horizontal, Vdd and Ground busses are metal, 4L wide. Clock connections are poly, 2L wide.
Approximate Power Consumption: 86.7 pW

Cifplot

(SEE NEXT PAGE)

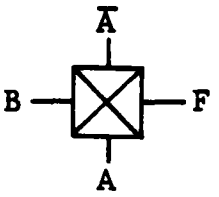
Pla Clock In (PlaClkIn)



Standard Cell: PlaClkOut CIF ID: 960

Description: Pla clock out cell used on every odd output term. Tessellates directly with PlaClkOut2, which is used at every even output term of the Pla. Both provide a clocked Pla output and require two inputs: inverted and noninverted PHI2 clock signal.

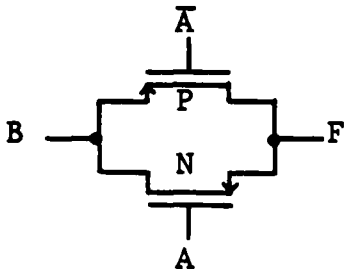
Logic Symbol



Truth Table

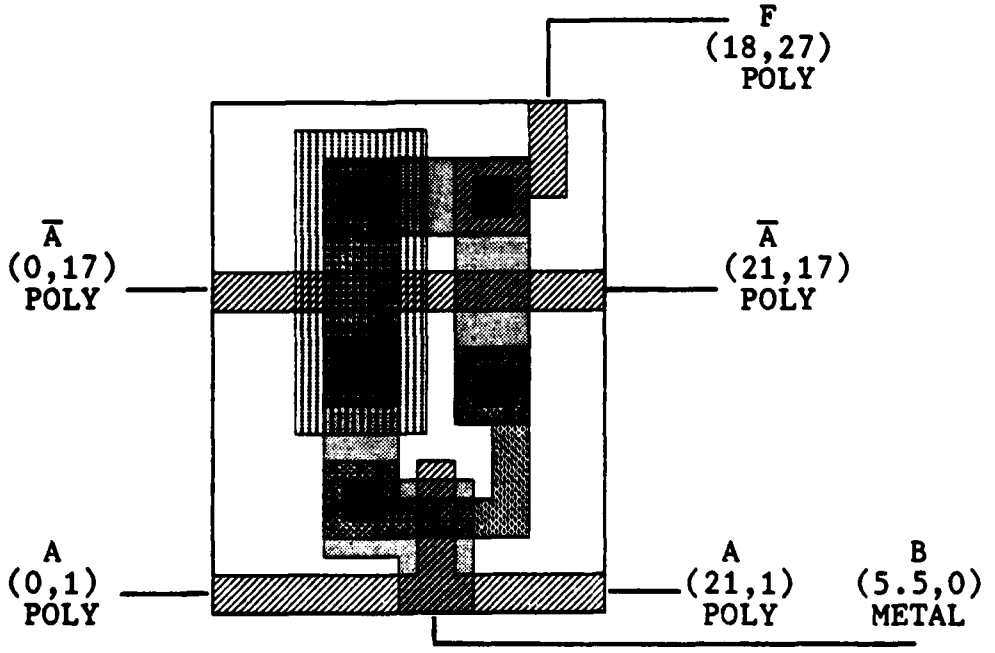
A	$\overline{A}$	B	F
0	1	0	X
1	0	0	0
0	1	1	X
1	0	1	1

Schematic



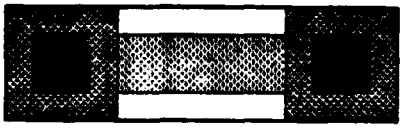
Size: Width = 13L Length = 27L
Tesselation: horizontal, poly,2L wide, 16L separation
Approximate Power Consumption: 52 pW

Cifplot

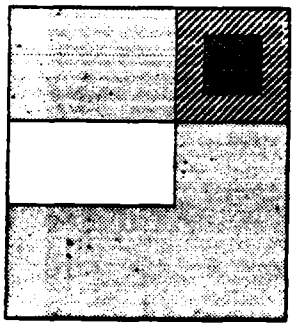


Pla Cells

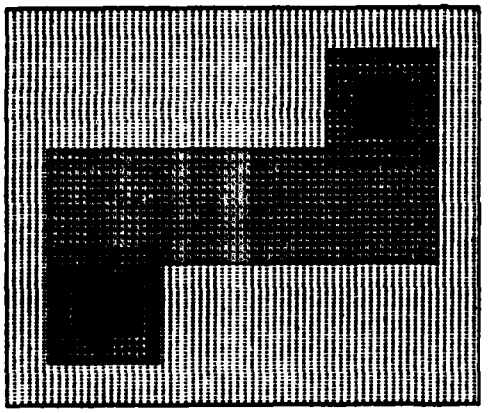
The following pages of Appendix B contain CIFPLOTs of all PLA cells used in the CMOS/SOS PLA generator written for this thesis. Cells are identified only by CIF name and symbol number. Where possible, coordinates as well as layers are labeled. PLA cells use CIF numbers 962 through 974. These numbers should not be used for other CMOS/SOS cells or for a PLA used in a CMOS/SOS design.



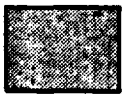
NMOS Cell (NMOS)
CIF #: 962
Size: 14L x 4L



Pla Connect (CCONNE1)
CIF #: 963
Size: 10L x 7L

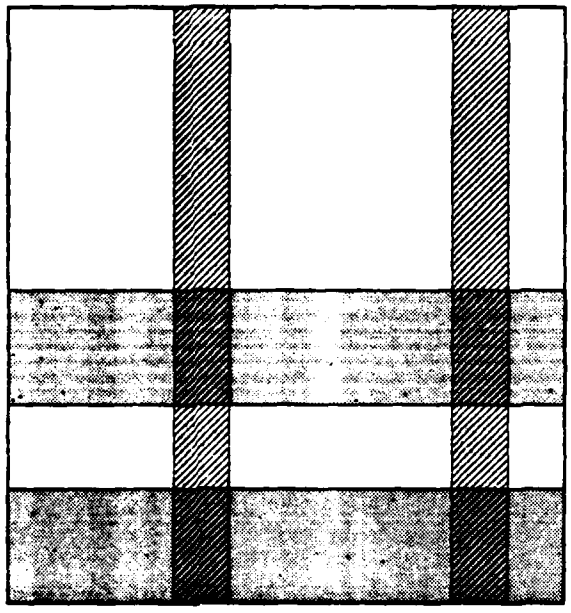


PMOS Cell (PMOS)
CIF #: 964
Size: 17L x 14L

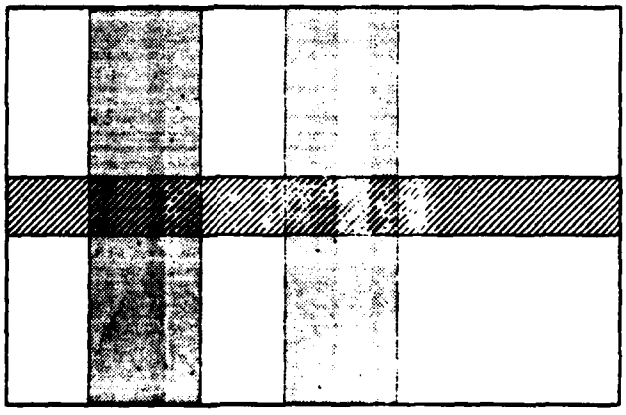


Pla Ground Connect (CGNDCON)
CIF #: 965
Size: 4L x 3L

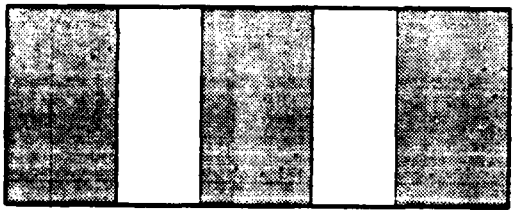
NMOS Space (NSPACE)
CIF #: 966
Size: 13L x 4L



Pla Cell Left (CCELL)
CIF #: 967
Size: 20L x 21L

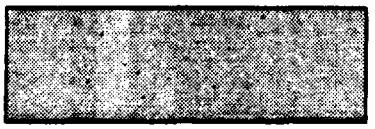


Pla Cell Right (CCELLR)
CIF #: 968
Size: 22L x 14L

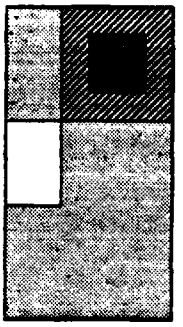


Pla Cell Space (CCELLSP)
CIF #: 969
Size: 18L x 7L

Pla Out (PlaOut)
CIf#; 971
Size: 2L x 7L



Pla Connect 2 (CCONNE2)
CIF #: 970
Size: 14L x 4L



Pla Connect 3 (CCONNE3)
CIF #: 972
Size: 10L x 6L

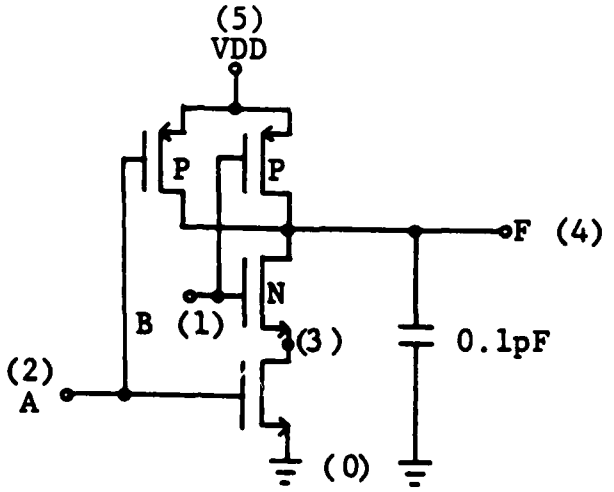
Pla Hole Space 1 (HOLESP1)
CIF#: 973
Size: 10L x 4L

Pla Hole Space 2 (HOLESP2)
CIF#: 974
Size: 6L x 4L

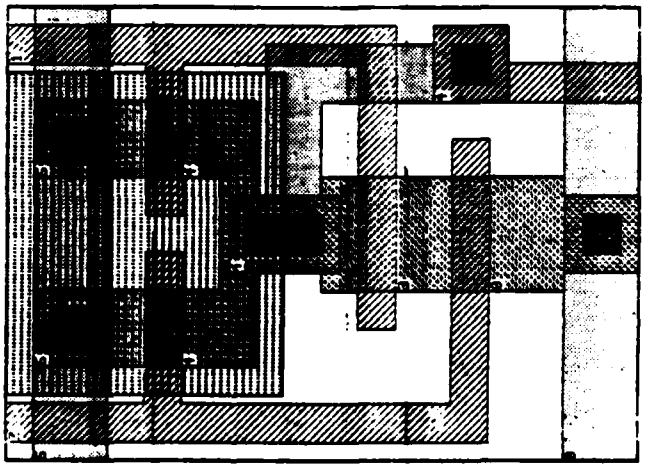
Appendix C

SPICE analyses are presented for the basic standard cells of the cell library. Certain standard cells, such as the PLA clock out cell, were not simulated because they incorporate other cells as subcells. In these instances, the approximate power consumption is the same as the combined power consumption of the subcells. Additionally, the PLA clock-out cell was not simulated because it is functionally identical to the transmission gate. All analysis results were as expected with the exception of the transmission gate. Difficulties were encountered in determining the correct MOSFET models, which resulted is less than ideal transient responses. The basic design of the transmission gate, however, is believed to be sound.

SPICE circuit models are presented for each different cell. Additionally, the CIFPLOT layout of each cell, with automatically numbered and labeled nodes, is included. Note: CIFPLOT does not normally number nodes sequentially. However, the files containing the node numbers "filename.nodes" were edited for each cell so node numbers are sequential.



(b) Schematic With Labeled Nodes



(a) Layout With Labeled Nodes

Figure C-1 Two Input NAND SPICE Model

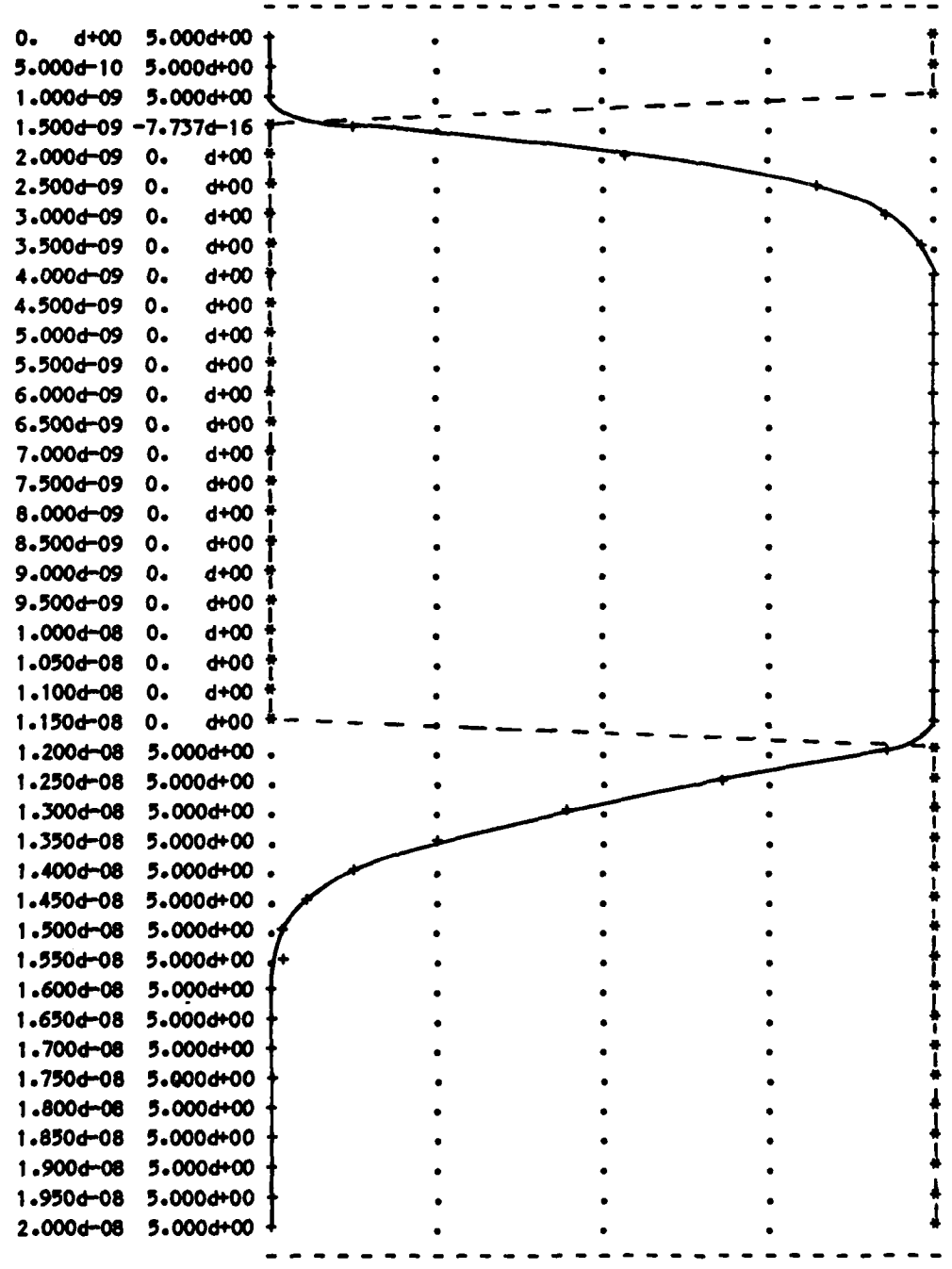
```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:11******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
+LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
+LEVEL=1
 VDD 5 0 DC 5V
 MPD1 4 1 3 0 N L=4UM W=12UM
 MPD2 3 2 0 0 N L=4UM W=12UM
 MPU1 4 2 5 5 P L=4UM W=8UM
 MPU2 4 1 5 5 P L=4UM W=8UM
 CDBK 4 0 0.1PF
 VIN1 1 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN2 2 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
```

A and B change from 5V to 0V to 5V

```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:11******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                 N          P
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000
```

```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:11******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 (  1)    5.0000    (  2)    5.0000    (  3)    0.0000    (  4)    0.0000

 (  5)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -1.387d-11

     VIN1      0.   d+00

     VIN2      0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:11******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0
0**** MOSFETS

0            MPD1       MPD2       MPU1       MPU2
0MODEL     N          N          P          P
 ID        1.39d-11   1.39d-11 -1.93d-12 -1.93d-12
 VGS         5.000      5.000      0.         0.
 VDS         0.000      0.000     -5.000     -5.000
 VBS        -0.000      0.         0.         0.

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:11******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
OLEGEND:

 *: V(1)
 +: V(4)
X
     TIME        V(1)

X(*+)————————— 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
 0.    d+00   5.000d+00
 5.000d-10    5.000d+00
 1.000d-09    5.000d+00
 1.500d-09   -7.737d-16
 2.000d-09    0.    d+00
 2.500d-09    0.    d+00
 3.000d-09    0.    d+00
 3.500d-09    0.    d+00
 4.000d-09    0.    d+00
 4.500d-09    0.    d+00
 5.000d-09    0.    d+00
 5.500d-09    0.    d+00
 6.000d-09    0.    d+00
 6.500d-09    0.    d+00
 7.000d-09    0.    d+00
 7.500d-09    0.    d+00
 8.000d-09    0.    d+00
 8.500d-09    0.    d+00
 9.000d-09    0.    d+00
 9.500d-09    0.    d+00
 1.000d-08    0.    d+00
 1.050d-08    0.    d+00
 1.100d-08    0.    d+00
 1.150d-08    0.    d+00
 1.200d-08    5.000d+00
 1.250d-08    5.000d+00
 1.300d-08    5.000d+00
 1.350d-08    5.000d+00
 1.400d-08    5.000d+00
 1.450d-08    5.000d+00
 1.500d-08    5.000d+00
 1.550d-08    5.000d+00
 1.600d-08    5.000d+00
 1.650d-08    5.000d+00
 1.700d-08    5.000d+00
 1.750d-08    5.000d+00
 1.800d-08    5.000d+00
 1.850d-08    5.000d+00
 1.900d-08    5.000d+00
 1.950d-08    5.000d+00
 2.000d-08    5.000d+00
```

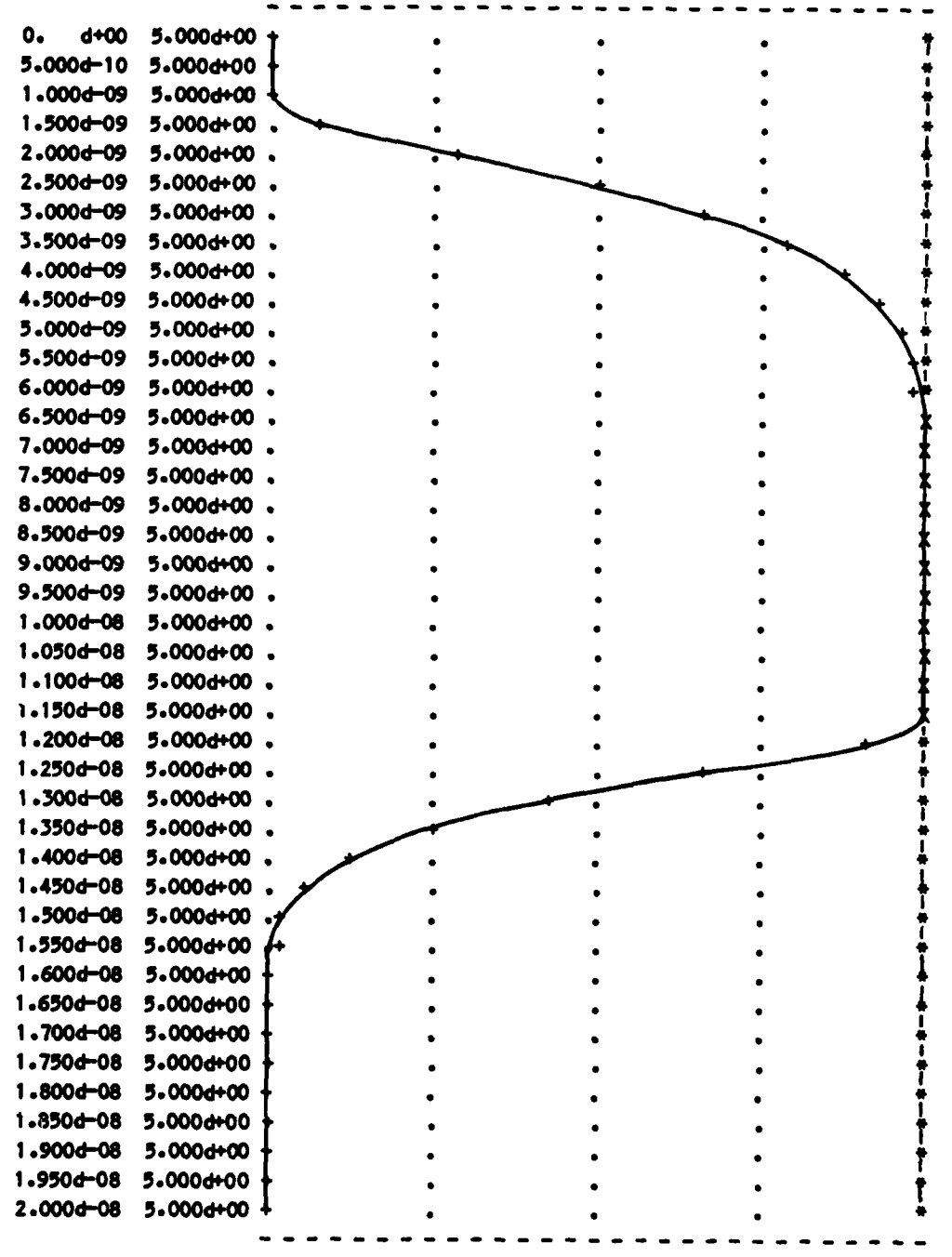
```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:34******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 5 0 DC 5V
 MPD1 4 1 3 0 N L=4UM W=12UM
 MPD2 3 2 0 0 N L=4UM W=12UM
 MPU1 4 2 5 5 P L=4UM W=8UM
 MPU2 4 1 5 5 P L=4UM W=8UM
 CDBK 4 0 0.1PF
 VIN1 1 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN2 2 0 PULSE (5V 5V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(2) V(4) (0V,5V)
 .END
```

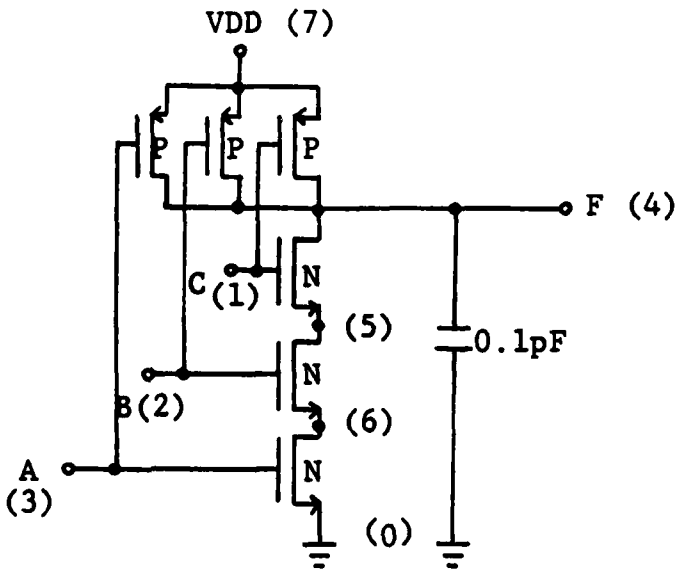
B changes as before.
A remains constant.

```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:34******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                 N          P
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000
```

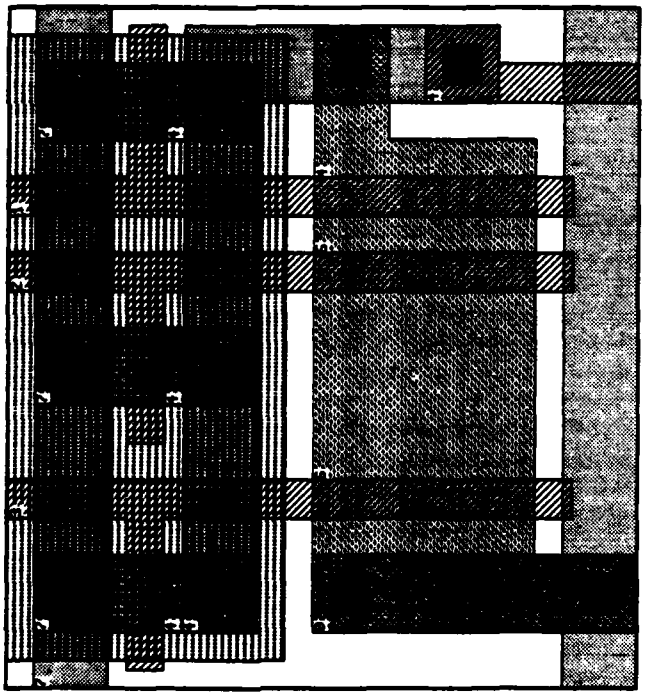
```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:34******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    0.0000    (  4)    0.0000

(  5)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -1.387d-11

     VIN1      0.   d+00

     VIN2      0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:34******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0
0**** MOSFETS

0            MPD1       MPD2       MPU1       MPU2
0MODEL     N          N          P          P
 ID        1.39d-11   1.39d-11 -1.93d-12 -1.93d-12
 VGS         5.000      5.000      0.         0.
 VDS         0.000      0.000     -5.000     -5.000
 VBS        -0.000      0.         0.         0.
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:11:34******

0       CMOS/SOS 2 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:1.5)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
OLEGEND:

 *: V(2)
 +: V(4)
X
     TIME        V(2)

X(*+)---------- 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```





(b) Schematic With Labeled Nodes



(a) Layout With Labeled Nodes

Figure C-2 Three Input NAND SPICE Model

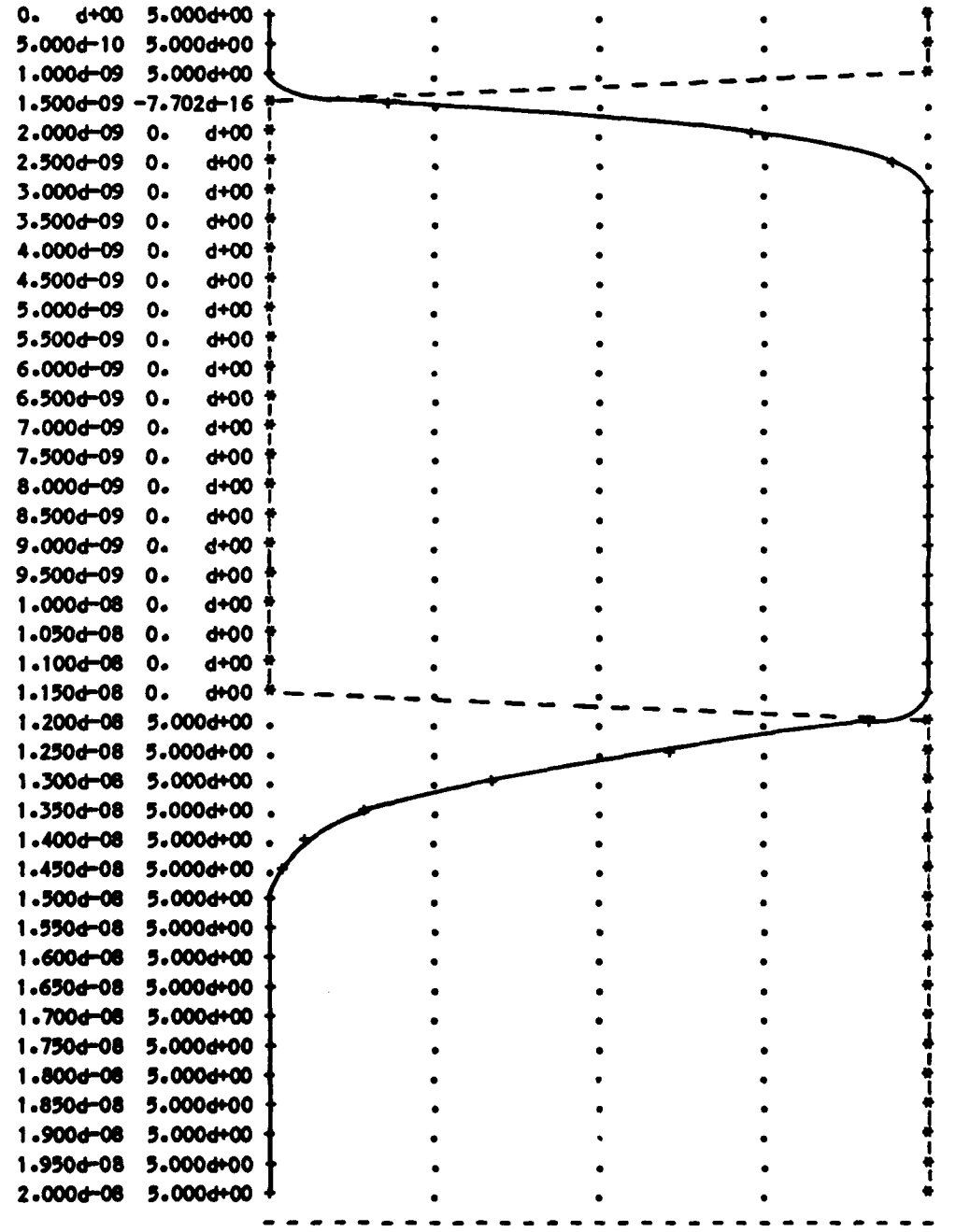
```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:45:37******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 7 0 DC 5V
 MPD1 4 1 5 0 N L=4UM W=24UM
 MPD2 5 2 6 0 N L=4UM W=24UM
 MPD3 6 3 0 0 N L=4UM W=24UM
 MPU1 4 3 7 7 P L=4UM W=8UM
 MPU2 4 2 7 7 P L=4UM W=8UM
 MPU3 4 1 7 7 P L=4UM W=8UM
 CDBK 4 0 0.1PF
 VIN1 1 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN2 2 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 VIN3 3 0 PULSE (5V 0V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
```

All inputs change from 5V to 0V to 5V

```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:45:37******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                 N          P
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000
```

```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:45:37******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 (  1)    5.0000    (  2)    5.0000    (  3)    5.0000    (  4)    0.0000

 (  5)    0.0000    (  6)    0.0000    (  7)    5.0000


     VOLTAGE SOURCE CURRENTS

     NAME        CURRENT

     VDD       -2.080d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3       0.   d+00


     TOTAL POWER DISSIPATION   1.04d-10  WATTS

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:45:37******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0
0**** MOSFETS

0             MPD1       MPD2       MPD3       MPU1       MPU2       MPU3
0MODEL      N          N          N          P          P          P
 ID         2.08d-11   2.08d-11   2.08d-11  -1.93d-12  -1.93d-12  -1.93d-12
 VGS          5.000      5.000      5.000      0.         0.         0.
 VDS          0.000      0.000      0.000     -5.000     -5.000     -5.000
 VBS         -0.000     -0.000      0.         0.         0.         0.

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:45:37******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)
0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
OLEGEND:

 *: V(1)
 +: V(4)
X
     TIME        V(1)

X(*+)————————— 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
  0.    d+00   5.000d+00
  5.000d-10    5.000d+00
  1.000d-09    5.000d+00
  1.500d-09   -7.702d-16
  2.000d-09    0.    d+00
  2.500d-09    0.    d+00
  3.000d-09    0.    d+00
  3.500d-09    0.    d+00
  4.000d-09    0.    d+00
  4.500d-09    0.    d+00
  5.000d-09    0.    d+00
  5.500d-09    0.    d+00
  6.000d-09    0.    d+00
  6.500d-09    0.    d+00
  7.000d-09    0.    d+00
  7.500d-09    0.    d+00
  8.000d-09    0.    d+00
  8.500d-09    0.    d+00
  9.000d-09    0.    d+00
  9.500d-09    0.    d+00
  1.000d-08    0.    d+00
  1.050d-08    0.    d+00
  1.100d-08    0.    d+00
  1.150d-08    0.    d+00
  1.200d-08    5.000d+00
  1.250d-08    5.000d+00
  1.300d-08    5.000d+00
  1.350d-08    5.000d+00
  1.400d-08    5.000d+00
  1.450d-08    5.000d+00
  1.500d-08    5.000d+00
  1.550d-08    5.000d+00
  1.600d-08    5.000d+00
  1.650d-08    5.000d+00
  1.700d-08    5.000d+00
  1.750d-08    5.000d+00
  1.800d-08    5.000d+00
  1.850d-08    5.000d+00
  1.900d-08    5.000d+00
  1.950d-08    5.000d+00
  2.000d-08    5.000d+00
```

```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:13:12******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0*****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 7 0 DC 5V
 MPD1 4 1 5 0 N L=4UM W=24UM
 MPD2 5 2 6 0 N L=4UM W=24UM
 MPD3 6 3 0 0 N L=4UM W=24UM
 MPU1 4 3 7 7 P L=4UM W=8UM
 MPU2 4 2 7 7 P L=4UM W=8UM
 MPU3 4 1 7 7 P L=4UM W=8UM
 CDBK 4 0 0.1PF
 VIN1 1 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN2 2 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN3 3 0 PULSE (5V 5V 1NS ONS ONS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
```

B and C change as before.
A remains constant.

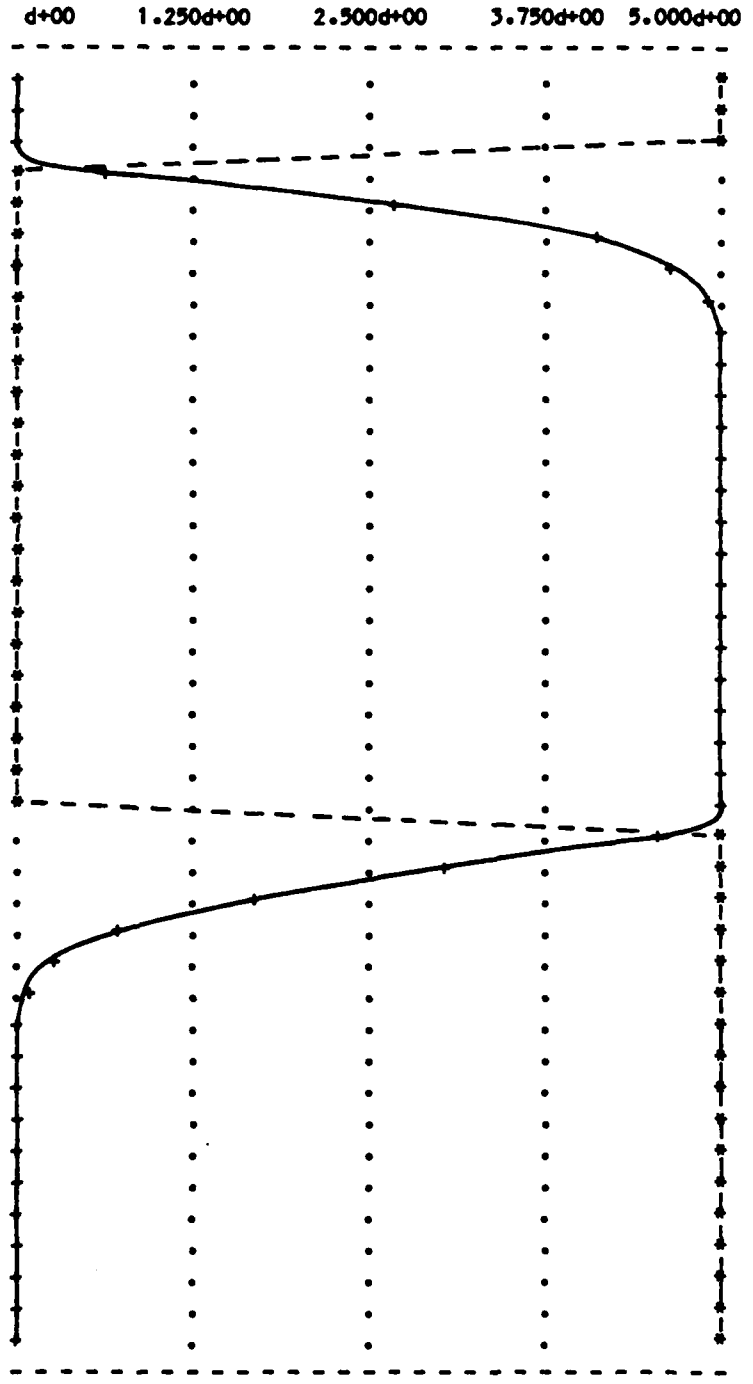
```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:13:12******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0*****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                N          P
0TYPE           NMOS       PMOS
0LEVEL            1.000      1.000
0VTO              1.000     -1.000
0KP            1.84d-05   9.21d-06
0GAMMA            1.979      0.685
0PHI              0.743      0.633
0CJ            5.09d-04   1.76d-04
0TOX           7.50d-08   7.50d-08
0NSUB          2.50d+16   3.00d+15
0LD            7.00d-07   7.00d-07
0UO             400.000    200.000
```

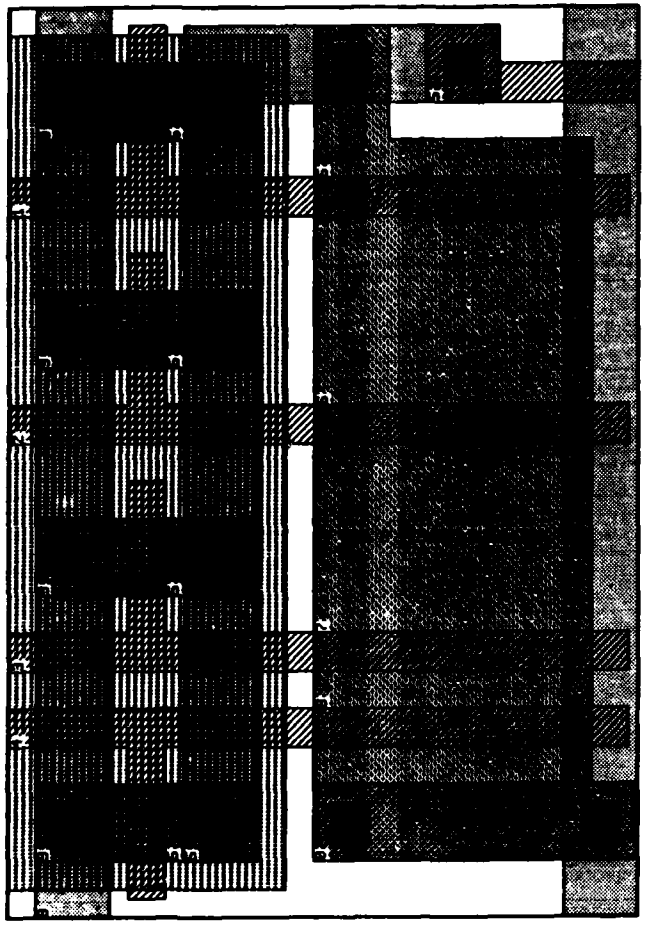
```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:13:12******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    5.0000    (  4)    0.0000

(  5)    0.0000    (  6)    0.0000    (  7)    5.0000


     VOLTAGE SOURCE CURRENTS

     NAME        CURRENT

     VDD       -2.080d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3       0.   d+00


     TOTAL POWER DISSIPATION   1.04d-10  WATTS

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:13:12******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0
0**** MOSFETS

0             MPD1       MPD2       MPD3       MPU1       MPU2       MPU3
OMODEL      N          N          N          P          P          P
 ID         2.08d-11   2.08d-11   2.08d-11  -1.93d-12  -1.93d-12  -1.93d-12
 VGS          5.000      5.000      5.000      0.         0.         0.
 VDS          0.000      0.000      0.000     -5.000     -5.000     -5.000
 VBS         -0.000     -0.000      0.         0.         0.         0.

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:13:12******

0       CMOS/SOS 3 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3)
0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

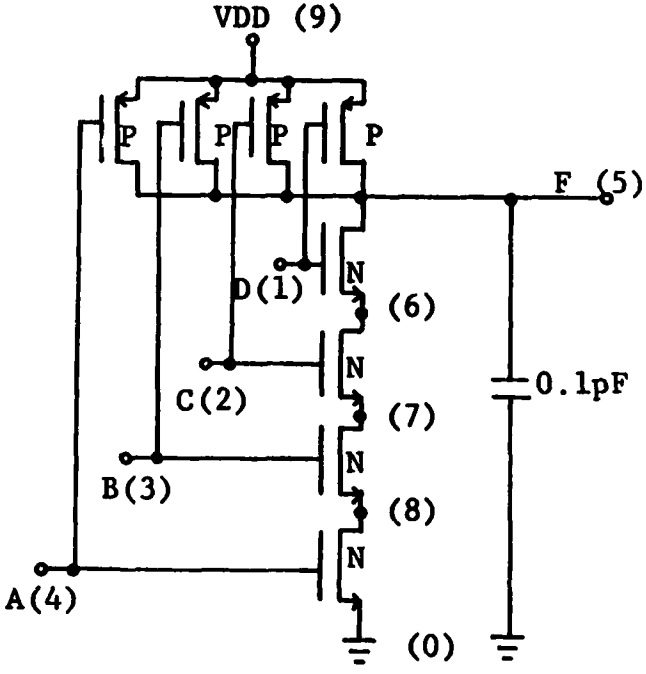
*: V(1)
+: V(4)
X

TIME	V(1)
0. d+00	5.000d+00
5.000d-10	5.000d+00
1.000d-09	5.000d+00
1.500d-09	-7.754d-16
2.000d-09	0. d+00
2.500d-09	0. d+00
3.000d-09	0. d+00
3.500d-09	0. d+00
4.000d-09	0. d+00
4.500d-09	0. d+00
5.000d-09	0. d+00
5.500d-09	0. d+00
6.000d-09	0. d+00
6.500d-09	0. d+00
7.000d-09	0. d+00
7.500d-09	0. d+00
8.000d-09	0. d+00
8.500d-09	0. d+00
9.000d-09	0. d+00
9.500d-09	0. d+00
1.000d-08	0. d+00
1.050d-08	0. d+00
1.100d-08	0. d+00
1.150d-08	0. d+00
1.200d-08	5.000d+00
1.250d-08	5.000d+00
1.300d-08	5.000d+00
1.350d-08	5.000d+00
1.400d-08	5.000d+00
1.450d-08	5.000d+00
1.500d-08	5.000d+00
1.550d-08	5.000d+00
1.600d-08	5.000d+00
1.650d-08	5.000d+00
1.700d-08	5.000d+00
1.750d-08	5.000d+00
1.800d-08	5.000d+00
1.850d-08	5.000d+00
1.900d-08	5.000d+00
1.950d-08	5.000d+00
2.000d-08	5.000d+00





(a) Layout With Labeled Nodes



(b) Schematic With Labeled Nodes

Figure C-3 Four Input NAND SPICE Model

```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:16:53*****

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 9 0 DC 5V
 MPD1 5 1 6 0 N L=4UM W=30UM
 MPD2 6 2 7 0 N L=4UM W=30UM
 MPD3 7 3 8 0 N L=4UM W=30UM
 MPD4 8 4 0 0 N L=4UM W=30UM
 MPU1 5 4 9 9 P L=4UM W=8UM
 MPU2 5 3 9 9 P L=4UM W=8UM
 MPU3 5 2 9 9 P L=4UM W=8UM
 MPU4 5 1 9 9 P L=4UM W=8UM
 CDBK 5 0 0.1PF
 VIN1 1 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN2 2 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN3 3 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN4 4 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(5) (0V,5V)
 .END
```

All inputs change from 5V to 0V to 5V.

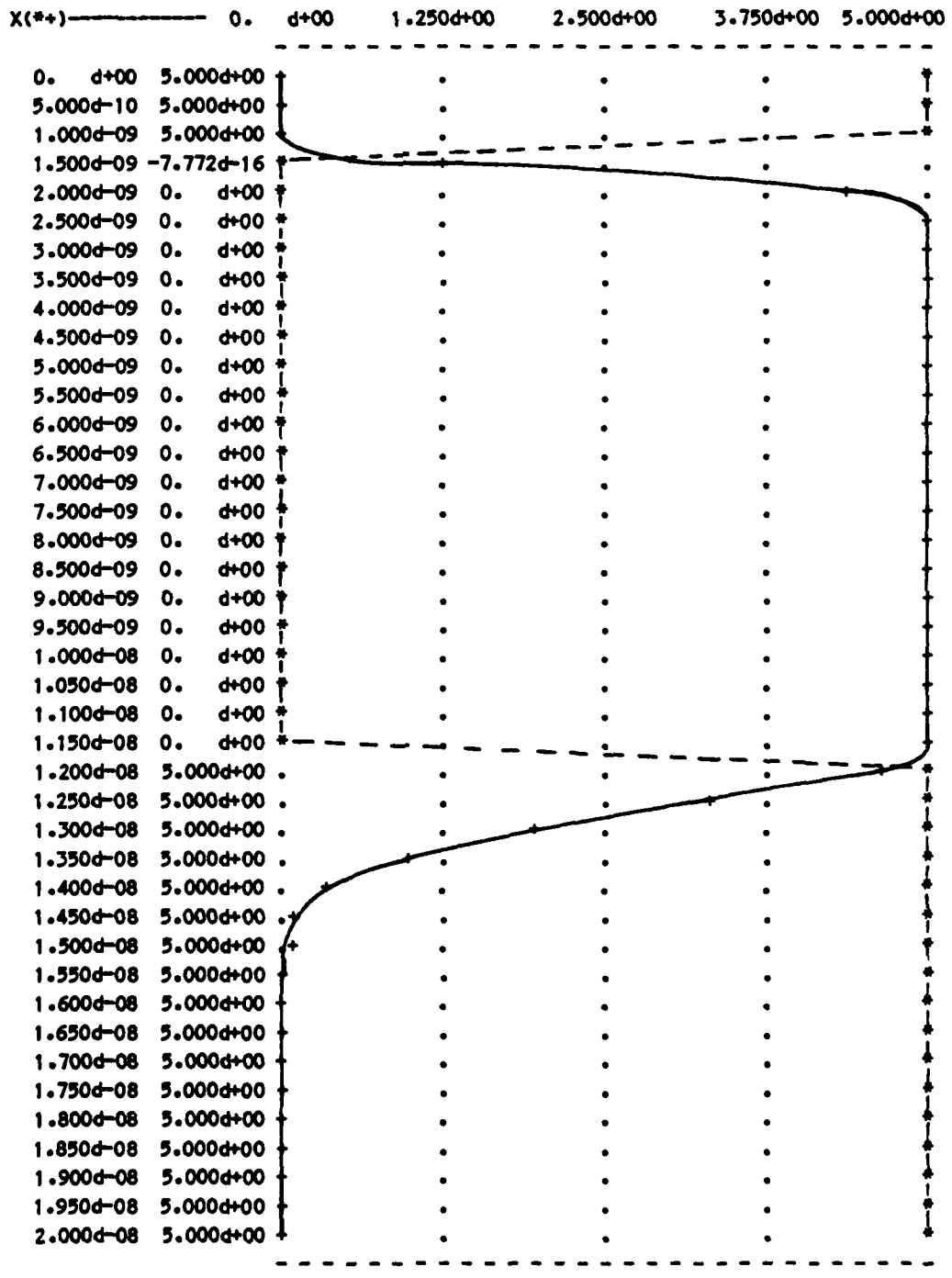
```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:16:53*****

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0*****    MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
                N          P
0TYPE           NMOS       PMOS
0LEVEL           1.000      1.000
0VTO             1.000     -1.000
0KP           1.84d-05   9.21d-06
0GAMMA           1.979      0.685
0PHI             0.743      0.633
0CJ           5.09d-04   1.76d-04
0TOX          7.50d-08   7.50d-08
0NSUB         2.50d+16   3.00d+15
0LD           7.00d-07   7.00d-07
0UO            400.000    200.000

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:16:53******

0        CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****      INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    5.0000    (  4)    5.0000

(  5)    0.0000    (  6)    0.0000    (  7)    0.0000    (  8)    0.0000

(  9)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME         CURRENT

     VDD       -2.773d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3       0.   d+00

     VIN4       0.   d+00

     TOTAL POWER DISSIPATION   1.39d-10  WATTS
```

```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:16:53******

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1       MPD2       MPD3       MPD4       MPU1       MPU2       MPU3
OMODEL     N          N          N          N          P          P          P
 ID        2.77d-11   2.77d-11   2.77d-11   2.76d-11  -1.93d-12  -1.93d-12  -1.93d-12
 VGS          5.000      5.000      5.000      5.000      0.         0.         0.
 VDS          0.000      0.000      0.000      0.000     -5.000     -5.000     -5.000
 VBS         -0.000     -0.000     -0.000      0.         0.         0.         0.


0            MPU4
OMODEL     P
 ID        -1.93d-12
 VGS          0.
 VDS         -5.000
 VBS          0.


1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:16:53******

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

*: V(1)
+: V(5)
X
TIME V(1)



```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:19:13*****

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 9 0 DC 5V
 MPD1 5 1 6 0 N L=4UM W=30UM
 MPD2 6 2 7 0 N L=4UM W=30UM
 MPD3 7 3 8 0 N L=4UM W=30UM
 MPD4 8 4 0 0 N L=4UM W=30UM
 MPU1 5 4 9 9 P L=4UM W=8UM
 MPU2 5 3 9 9 P L=4UM W=8UM
 MPU3 5 2 9 9 P L=4UM W=8UM
 MPU4 5 1 9 9 P L=4UM W=8UM
 CDBK 5 0 0.1PF
 VIN1 1 0 PULSE (5V 5V 1NS ONS ONS 10NS)
 VIN2 2 0 PULSE (5V 5V 1NS ONS ONS 10NS)
 VIN3 3 0 PULSE (5V 0V 1NS ONS ONS 10NS)
 VIN4 4 0 PULSE (5V 5V 1NS ONS ONS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(3) V(5) (0V,5V)
 .END


1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:19:13*****

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

Only input B undergoes previous transition.

All other inputs remain constant.

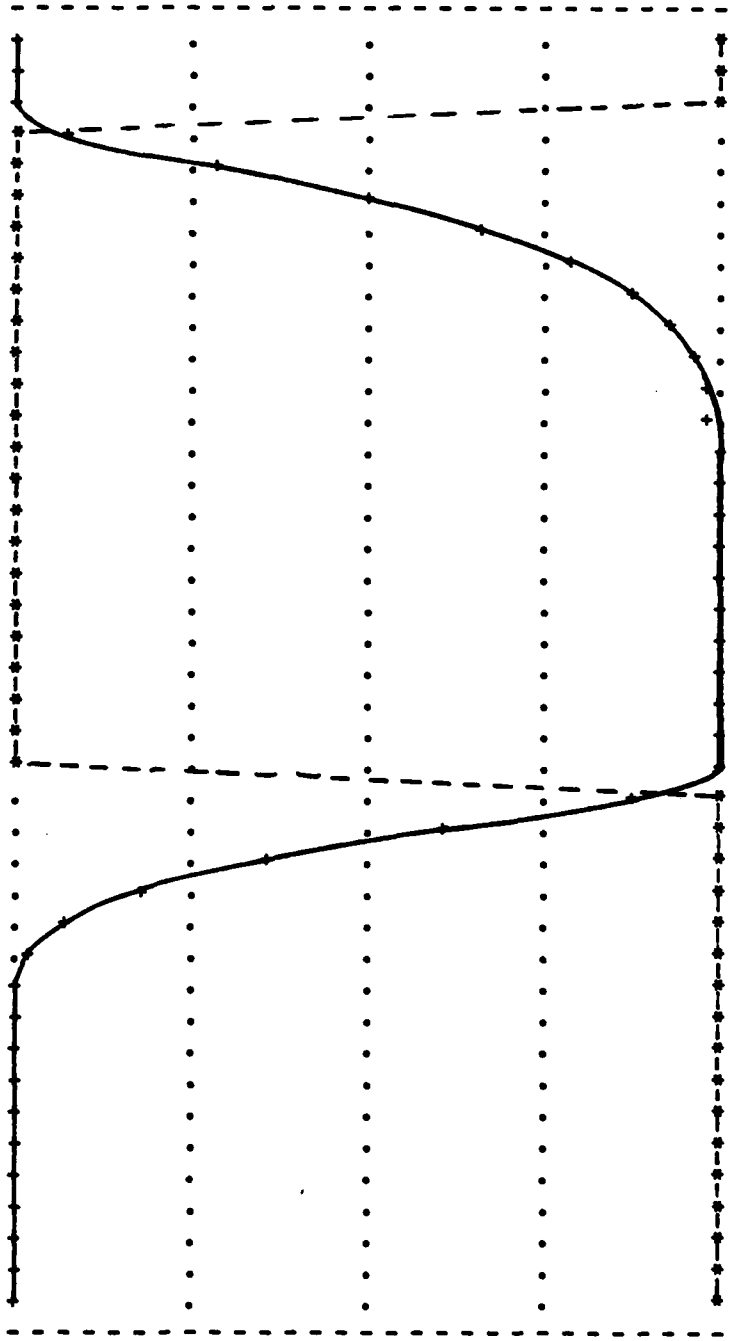
```
                N          P
0TYPE           NMOS       PMOS
0LEVEL           1.000      1.000
0VTO             1.000     -1.000
0KP           1.84d-05   9.21d-06
0GAMMA           1.979      0.685
0PHI             0.743      0.633
0CJ           5.09d-04   1.76d-04
0TOX          7.50d-08   7.50d-08
0NSUB         2.50d+16   3.00d+15
0LD           7.00d-07   7.00d-07
0UO            400.000    200.000

1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:19:13******

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****      INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    5.0000    (  4)    5.0000

(  5)    0.0000    (  6)    0.0000    (  7)    0.0000    (  8)    0.0000

(  9)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME         CURRENT

     VDD       -2.773d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3       0.   d+00

     VIN4       0.   d+00

     TOTAL POWER DISSIPATION   1.39d-10  WATTS
```

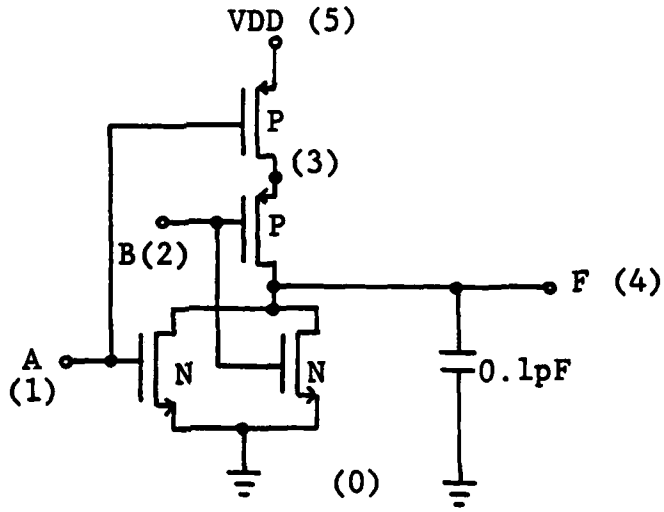
```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:19:13******

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1       MPD2       MPD3       MPD4       MPU1       MPU2       MPU3
0MODEL     N          N          N          N          P          P          P
 ID        2.77d-11   2.77d-11   2.77d-11   2.76d-11  -1.93d-12  -1.93d-12  -1.93d-12
 VGS          5.000      5.000      5.000      5.000      0.         0.         0.
 VDS          0.000      0.000      0.000      0.000     -5.000     -5.000     -5.000
 VBS         -0.000     -0.000     -0.000      0.         0.         0.         0.


0            MPU4
0MODEL     P
 ID        -1.93d-12
 VGS          0.
 VDS         -5.000
 VBS          0.


1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:19:13******

0       CMOS/SOS 4 INPUT NAND TRANSIENT ANALYSIS (W/L = 1:3.75)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

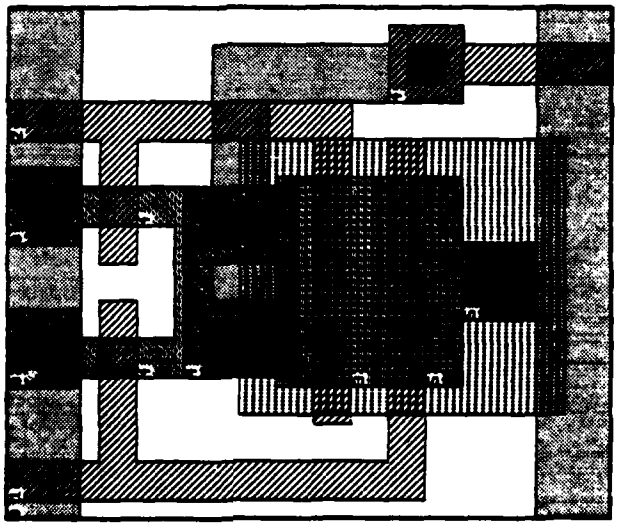
*: V(3)
+: V(5)
X

TIME	V(3)
X(*+)———— 0.	d+00 1.250d+00 2.500d+00 3.750d+00 5.000d+00
0. d+00	5.000d+00
5.000d-10	5.000d+00
1.000d-09	5.000d+00
1.500d-09	-7.772d-16
2.000d-09	0. d+00
2.500d-09	0. d+00
3.000d-09	0. d+00
3.500d-09	0. d+00
4.000d-09	0. d+00
4.500d-09	0. d+00
5.000d-09	0. d+00
5.500d-09	0. d+00
6.000d-09	0. d+00
6.500d-09	0. d+00
7.000d-09	0. d+00
7.500d-09	0. d+00
8.000d-09	0. d+00
8.500d-09	0. d+00
9.000d-09	0. d+00
9.500d-09	0. d+00
1.000d-08	0. d+00
1.050d-08	0. d+00
1.100d-08	0. d+00
1.150d-08	0. d+00
1.200d-08	5.000d+00
1.250d-08	5.000d+00
1.300d-08	5.000d+00
1.350d-08	5.000d+00
1.400d-08	5.000d+00
1.450d-08	5.000d+00
1.500d-08	5.000d+00
1.550d-08	5.000d+00
1.600d-08	5.000d+00
1.650d-08	5.000d+00
1.700d-08	5.000d+00
1.750d-08	5.000d+00
1.800d-08	5.000d+00
1.850d-08	5.000d+00
1.900d-08	5.000d+00
1.950d-08	5.000d+00
2.000d-08	5.000d+00





(b) Schematic With Labeled Nodes



(a) Layout With Labeled Nodes

Figure C-4 Two Input NOR SPICE Model

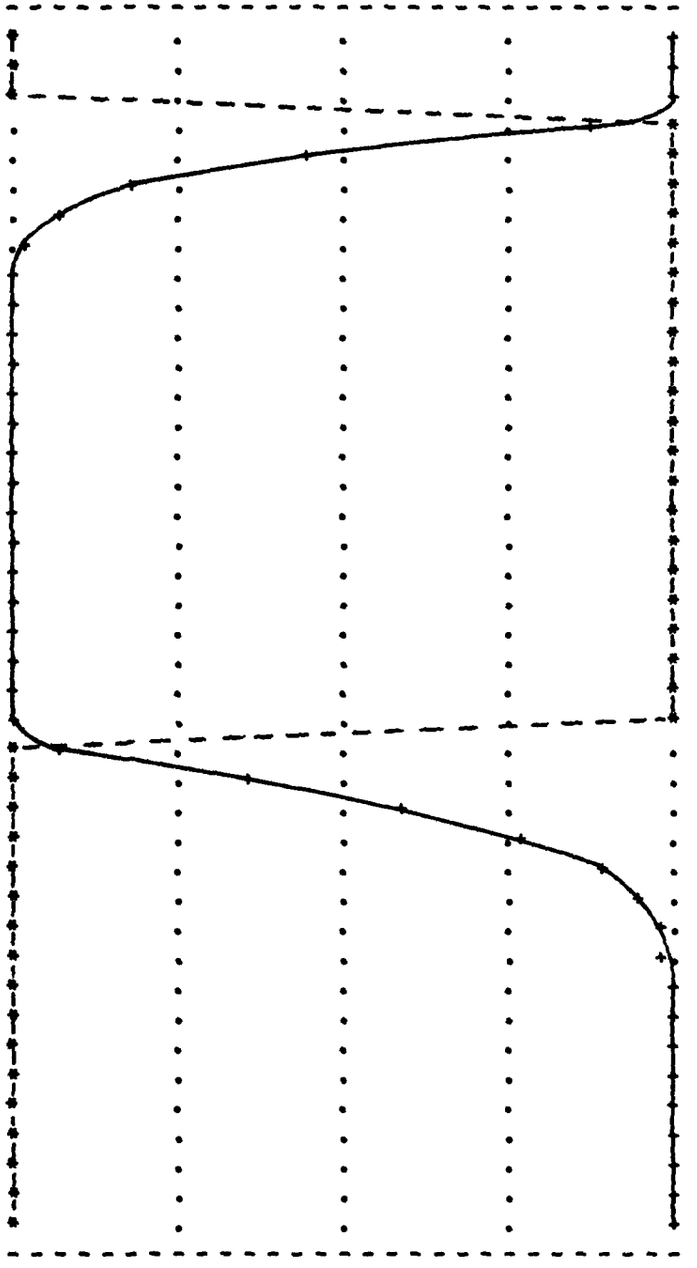
```
1*******08/20/83 ********  SPICE 2G.1 (15OCT80)  ********15:14:02******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 5 0 DC 5V
 MPD1 4 1 0 0 N L=4UM W=4UM
 MPD2 4 2 0 0 N L=4UM W=4UM
 MPU1 4 2 3 5 P L=4UM W=22UM
 MPU2 3 1 5 5 P L=4UM W=22UM
 CDBK 4 0 0.1PF
 VIN1 1 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)
 VIN2 2 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
```

Inputs A and B change from 0V to 5V to 0V.

```
1*******08/20/83 ********  SPICE 2G.1 (15OCT80)  ********15:14:02******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                 N          P
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000
```

```
1********08/20/83 ********  SPICE 2G.1 (15OCT80)  *********15:14:02******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    0.        (  2)    0.        (  3)    5.0000    (  4)    5.0000

(  5)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME        CURRENT

     VDD       -1.387d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1********08/20/83 ********  SPICE 2G.1 (15OCT80)  *********15:14:02******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0
0**** MOSFETS

0            MPD1       MPD2       MPU1       MPU2
0MODEL      N          N          P          P
 ID        1.93d-12   1.93d-12  -1.39d-11  -1.39d-11
 VGS         0.         0.        -5.000     -5.000
 VDS         5.000      5.000     -0.000     -0.000
 VBS         0.         0.         0.000      0.

1********08/20/83 ********  SPICE 2G.1 (15OCT80)  *********15:14:02******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
0LEGEND:

 *: V(1)
 +: V(4)

X
     TIME        V(1)

X(*+)————————— 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
  0.   d+00  0.   d+00
 5.000d-10   0.   d+00
 1.000d-09   0.   d+00
 1.500d-09   5.000d+00
 2.000d-09   5.000d+00
 2.500d-09   5.000d+00
 3.000d-09   5.000d+00
 3.500d-09   5.000d+00
 4.000d-09   5.000d+00
 4.500d-09   5.000d+00
 5.000d-09   5.000d+00
 5.500d-09   5.000d+00
 6.000d-09   5.000d+00
 6.500d-09   5.000d+00
 7.000d-09   5.000d+00
 7.500d-09   5.000d+00
 8.000d-09   5.000d+00
 8.500d-09   5.000d+00
 9.000d-09   5.000d+00
 9.500d-09   5.000d+00
 1.000d-08   5.000d+00
 1.050d-08   5.000d+00
 1.100d-08   5.000d+00
 1.150d-08   5.000d+00
 1.200d-08  -8.271d-15
 1.250d-08   0.   d+00
 1.300d-08   0.   d+00
 1.350d-08   0.   d+00
 1.400d-08   0.   d+00
 1.450d-08   0.   d+00
 1.500d-08   0.   d+00
 1.550d-08   0.   d+00
 1.600d-08   0.   d+00
 1.650d-08   0.   d+00
 1.700d-08   0.   d+00
 1.750d-08   0.   d+00
 1.800d-08   0.   d+00
 1.850d-08   0.   d+00
 1.900d-08   0.   d+00
 1.950d-08   0.   d+00
 2.000d-08   0.   d+00
```

```
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:22:39******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0*****************************************************************************


 .WIDTH OUT=80
 .OPTIONS ITL1=500 ITL5=0
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=1
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=1
 VDD 5 0 DC 5V
 MPD1 4 1 0 0 N L=4UM W=4UM
 MPD2 4 2 0 0 N L=4UM W=4UM
 MPU1 4 2 3 5 P L=4UM W=22UM
 MPU2 3 1 5 5 P L=4UM W=22UM
 CDBK 4 0 0.1PF
 VIN1 1 0 PULSE (0V 5V 1NS 0NS 0NS 10NS)
 VIN2 2 0 PULSE (0V 0V 1NS 0NS 0NS 10NS)
 .TRAN 0.5NS 20NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
1********10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:22:39******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0*****************************************************************************


                 N          P
0TYPE          NMOS       PMOS
0LEVEL        1.000      1.000
0VTO          1.000     -1.000
0KP        1.84d-05   9.21d-06
0GAMMA        1.979      0.685
0PHI          0.743      0.633
0CJ        5.09d-04   1.76d-04
0TOX       7.50d-08   7.50d-08
0NSUB      2.50d+16   3.00d+15
0LD        7.00d-07   7.00d-07
0UO         400.000    200.000
```

Input A undergoes same transition as before.

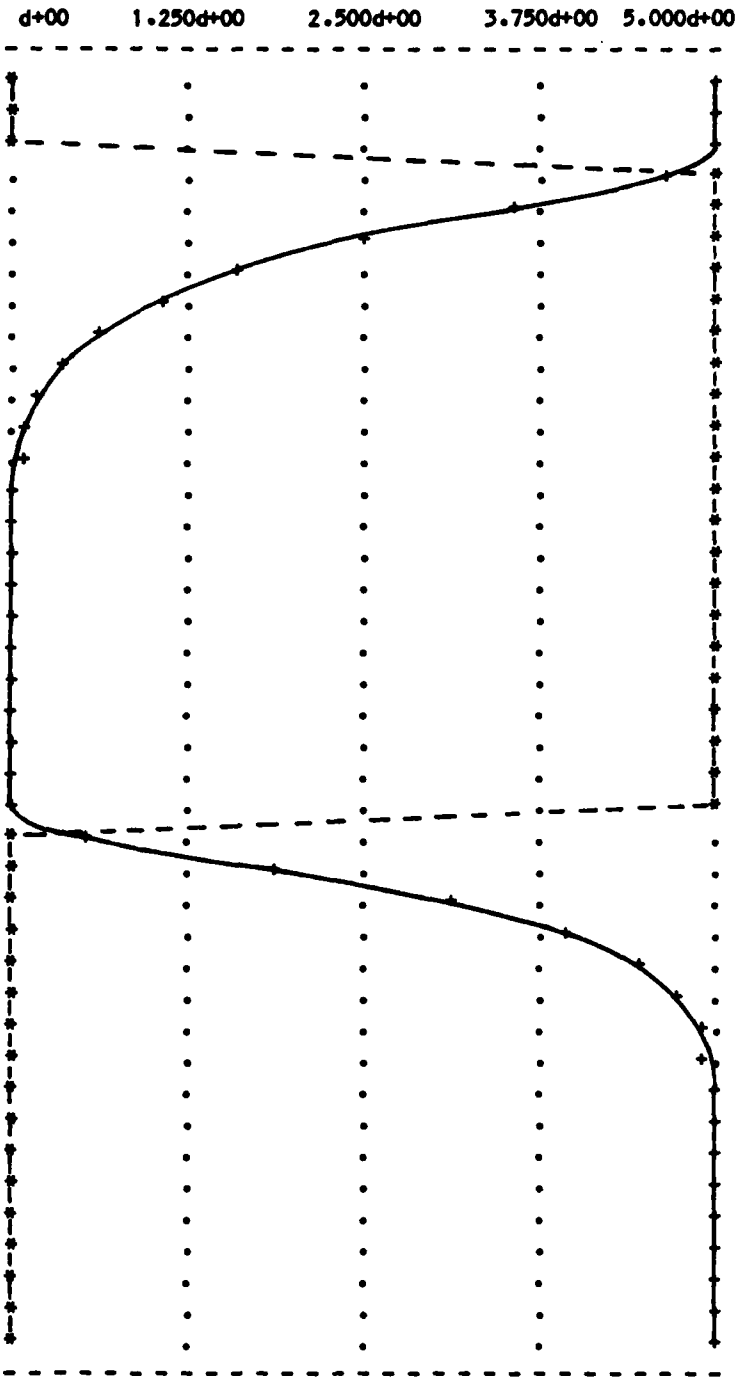
Input B remains constant 0V.

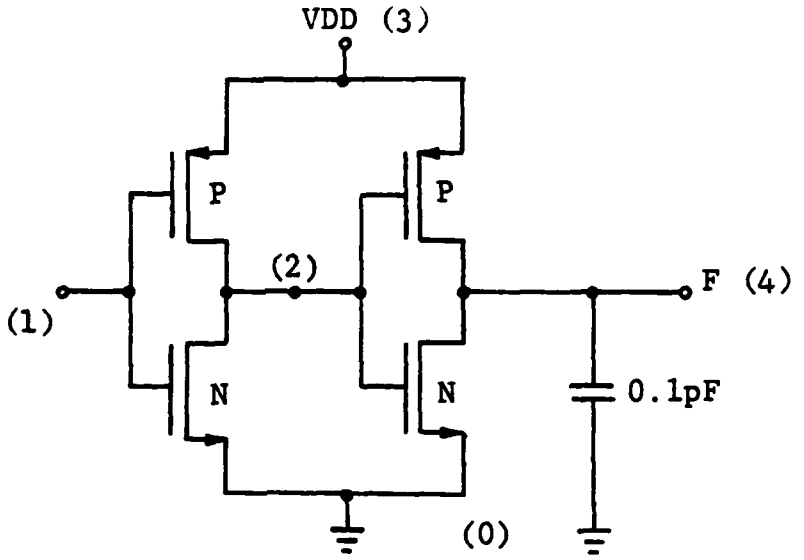
```
1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:22:39******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    0.        (  2)    0.        (  3)    5.0000    (  4)    5.0000

(  5)    5.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -1.387d-11

     VIN1      0.   d+00

     VIN2      0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:22:39******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************

0
0**** MOSFETS

0            MPD1       MPD2       MPU1       MPU2
0MODEL     N          N          P          P
 ID        1.93d-12   1.93d-12  -1.39d-11  -1.39d-11
 VGS         0.         0.        -5.000     -5.000
 VDS         5.000      5.000     -0.000     -0.000
 VBS         0.         0.         0.000      0.

1*******10/02/83 ********  SPICE 2G.1 (15OCT80)  ********20:22:39******

0       CMOS/SOS 2 INPUT NOR TRANSIENT ANALYSIS (W/L = 5.5:1)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

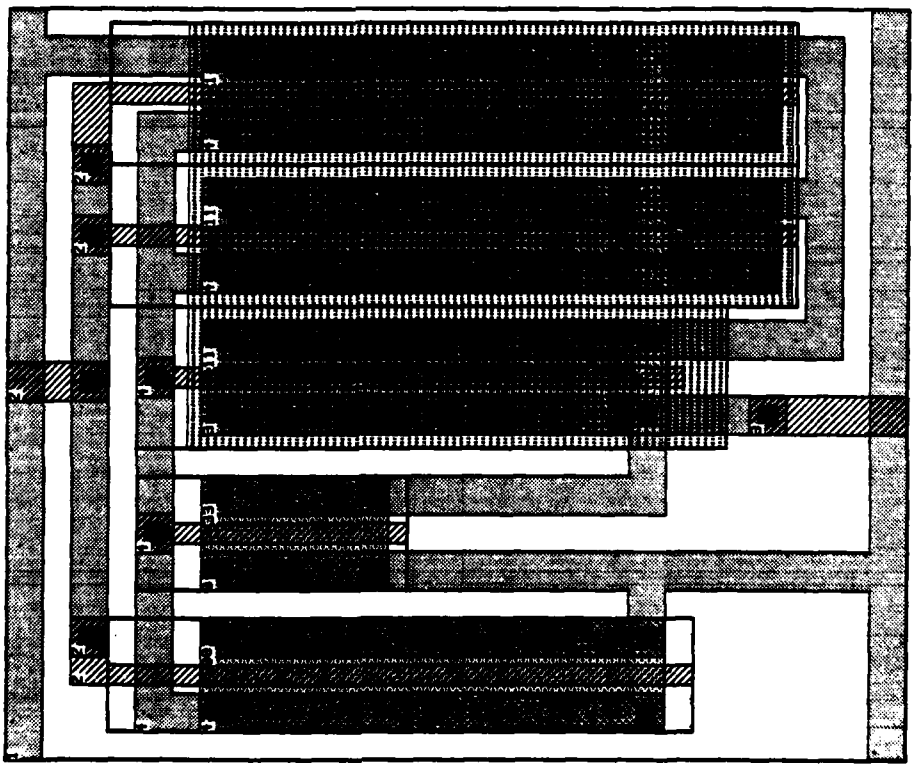
*: V(1)
+: V(4)
X

TIME	V(1)
0. d+00	0. d+00
5.000d-10	0. d+00
1.000d-09	0. d+00
1.500d-09	5.000d+00
2.000d-09	5.000d+00
2.500d-09	5.000d+00
3.000d-09	5.000d+00
3.500d-09	5.000d+00
4.000d-09	5.000d+00
4.500d-09	5.000d+00
5.000d-09	5.000d+00
5.500d-09	5.000d+00
6.000d-09	5.000d+00
6.500d-09	5.000d+00
7.000d-09	5.000d+00
7.500d-09	5.000d+00
8.000d-09	5.000d+00
8.500d-09	5.000d+00
9.000d-09	5.000d+00
9.500d-09	5.000d+00
1.000d-08	5.000d+00
1.050d-08	5.000d+00
1.100d-08	5.000d+00
1.150d-08	5.000d+00
1.200d-08	-8.271d-15
1.250d-08	0. d+00
1.300d-08	0. d+00
1.350d-08	0. d+00
1.400d-08	0. d+00
1.450d-08	0. d+00
1.500d-08	0. d+00
1.550d-08	0. d+00
1.600d-08	0. d+00
1.650d-08	0. d+00
1.700d-08	0. d+00
1.750d-08	0. d+00
1.800d-08	0. d+00
1.850d-08	0. d+00
1.900d-08	0. d+00
1.950d-08	0. d+00
2.000d-08	0. d+00





(a) Schematic With Labeled Nodes



(b) Layout With Labeled Nodes

Figure C-5 Double Buffered Output SPICE Model

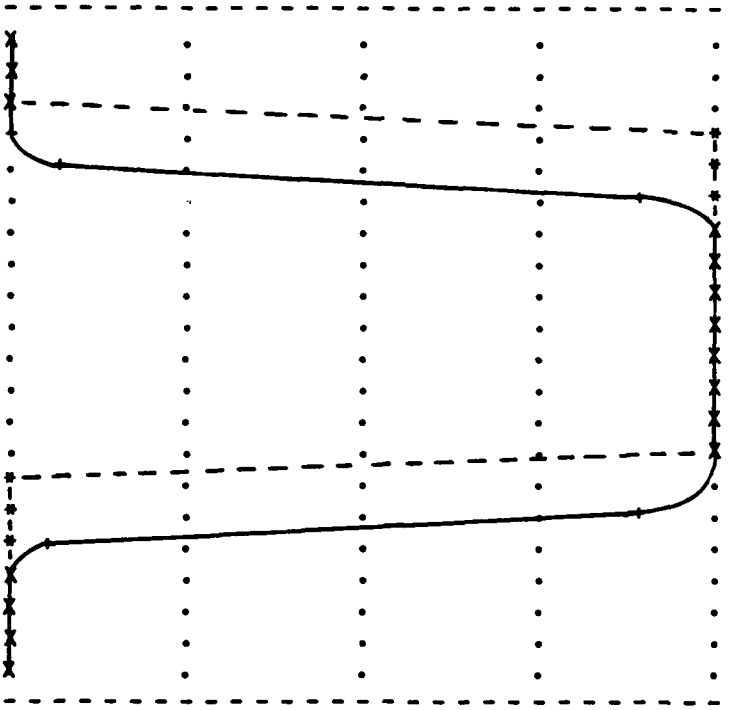
```
1********09/24/83 ********  SPICE 2G.1 (15OCT80)  ********20:49:03*****

0        CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=3
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=3
 VDD 3 0 DC 5V
 MPD1 2 1 0 0 N L=4UM W=40UM
 MPU1 2 1 3 3 P L=4UM W=100UM
 MPD2 4 2 0 0 N L=4UM W=100UM
 MPU2 4 2 3 3 P L=4UM W=250UM
 CDBK 4 0 0.1PF
 VIN 1 0 PULSE (0V 5V 1.0NS 0NS 0NS 5NS)
 .TRAN 0.5NS 10.0NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
```

Input changes from 0V to 5V to 0V.

```
1********09/24/83 ********  SPICE 2G.1 (15OCT80)  ********20:49:03*****

0        CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                 N          P
0TYPE            NMOS       PMOS
0LEVEL             3.000      3.000
0VTO               1.000     -1.000
0KP             1.84d-05   9.21d-06
0GAMMA             1.979      0.685
0PHI               0.743      0.633
0CJ             5.09d-04   1.76d-04
0TOX            7.50d-08   7.50d-08
0NSUB           2.50d+16   3.00d+15
0LD             7.00d-07   7.00d-07
0UO              400.000    200.000
0THETA             0.         0.
0ETA               0.         0.
0KAPPA             0.200      0.200
```

```
1*******09/24/83 ********  SPICE 2G.1 (15OCT80)  ********20:49:03*****

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

 (  1)    0.        (  2)    5.0000    (  3)    5.0000    (  4)    0.0000

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -1.387d-11

     VIN       0.   d+00

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1*******09/24/83 ********  SPICE 2G.1 (15OCT80)  ********20:49:03*****

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0******************************************************************************


0
0**** MOSFETS

0            MPD1       MPU1       MPD2       MPU2
OMODEL     N          P          N          P
 ID        1.93d-12 -6.93d-12  6.93d-12 -1.93d-12
 VGS         0.       -5.000     5.000    -0.000
 VDS         5.000    -0.000     0.000    -5.000
 VBS         0.        0.        0.        0.
1*******09/24/83 ********  SPICE 2G.1 (15OCT80)  ********20:49:03*****

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
OLEGEND:

 *: V(1)
 +: V(4)
X
     TIME        V(1)

X(*+)---------- 0.    d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



0. d+00	0. d+00
5.000d-10	0. d+00
1.000d-09	0. d+00
1.500d-09	5.000d+00
2.000d-09	5.000d+00
2.500d-09	5.000d+00
3.000d-09	5.000d+00
3.500d-09	5.000d+00
4.000d-09	5.000d+00
4.500d-09	5.000d+00
5.000d-09	5.000d+00
5.500d-09	5.000d+00
6.000d-09	5.000d+00
6.500d-09	5.000d+00
7.000d-09	-4.136d-15
7.500d-09	0. d+00
8.000d-09	0. d+00
8.500d-09	0. d+00
9.000d-09	0. d+00
9.500d-09	0. d+00
1.000d-08	0. d+00

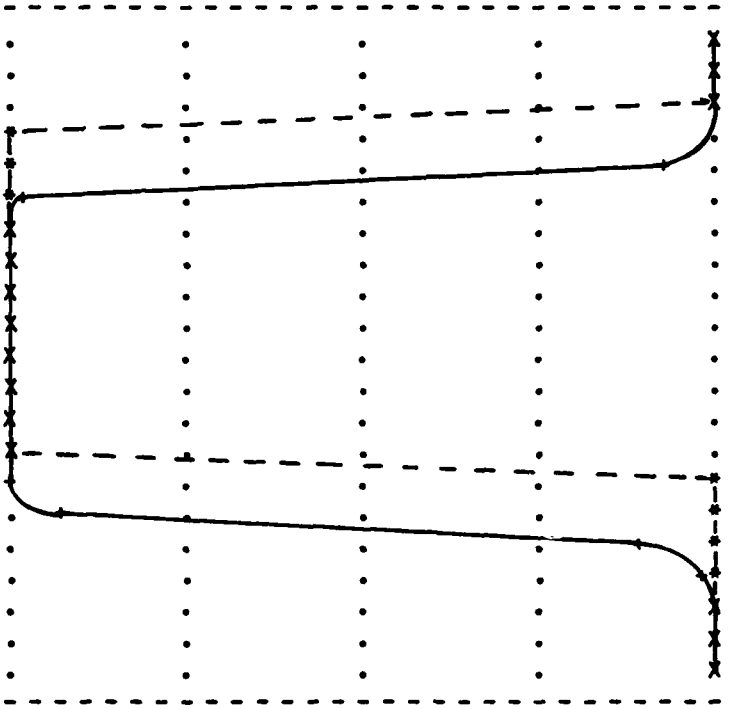
```
1********09/29/83 ********  SPICE 2G.1 (15OCT80)  ********16:30:57******

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****      INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0*****************************************************************************


 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=3
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=3
 VDD 3 0 DC 5V
 MPD1 2 1 0 0 N L=4UM W=40UM
 MPU1 2 1 3 3 P L=4UM W=100UM
 MPD2 4 2 0 0 N L=4UM W=100UM
 MPU2 4 2 3 3 P L=4UM W=250UM
 CDBK 4 0 0.1PF
 VIN 1 0 PULSE (5V 0V 1.0NS 0NS 0NS 5NS)
 .TRAN 0.5NS 10.0NS
 .PLOT TRAN V(1) V(4) (0V,5V)
 .END
```

Input changes from 5V to 0V to 5V.

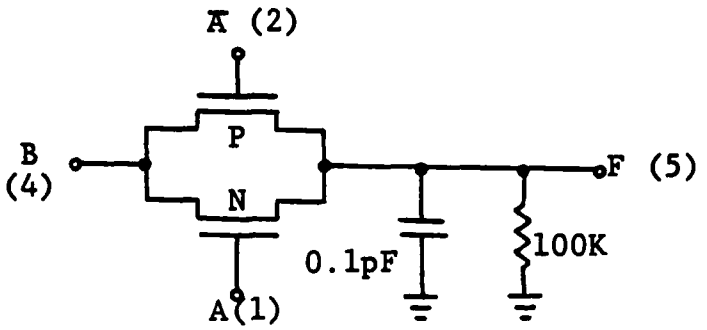
```
1********09/29/83 ********  SPICE 2G.1 (15OCT80)  ********16:30:57******

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****      MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0*****************************************************************************


                N          P
0TYPE           NMOS       PMOS
0LEVEL           3.000      3.000
0VTO             1.000     -1.000
0KP           1.84d-05   9.21d-06
0GAMMA           1.979      0.685
0PHI             0.743      0.633
0CJ           5.09d-04   1.76d-04
0TOX          7.50d-08   7.50d-08
0NSUB         2.50d+16   3.00d+15
0LD           7.00d-07   7.00d-07
0UO            400.000    200.000
0THETA           0.         0.
0ETA             0.         0.
0KAPPA           0.200      0.200
```

```
1********09/29/83 ********  SPICE 2G.1 (15OCT80)  ********16:30:57*****

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    0.0000 -  (  3)    5.0000    (  4)    5.0000

    VOLTAGE SOURCE CURRENTS

    NAME       CURRENT

    VDD      -1.387d-11

    VIN       0.   d+00

    TOTAL POWER DISSIPATION   6.93d-11  WATTS

1********09/29/83 ********  SPICE 2G.1 (15OCT80)  ********16:30:57*****

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS

0            MPD1      MPU1      MPD2      MPU2
0MODEL     N         P         N         P
 ID        6.93d-12 -1.93d-12  1.93d-12 -6.93d-12
 VGS          5.000     0.        0.000    -5.000
 VDS          0.000    -5.000     5.000    -0.000
 VBS          0.        0.        0.        0.
1********09/29/83 ********  SPICE 2G.1 (15OCT80)  ********16:30:57*****

0       CMOS/SOS DOUBLE BUFFERED OUTPUT TRANSIENT ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

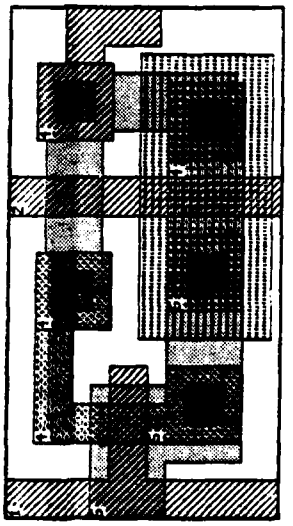
```
OLEGEND:

 *: V(1)
 +: V(4)
X
     TIME       V(1)

X(*+)---------- 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
  0.    d+00   5.000d+00 .
  5.000d-10    5.000d+00 .
  1.000d-09    5.000d+00 .
  1.500d-09    0.    d+00 *
  2.000d-09    0.    d+00 *
  2.500d-09    0.    d+00 *
  3.000d-09    0.    d+00 X
  3.500d-09    0.    d+00 X
  4.000d-09    0.    d+00 X
  4.500d-09    0.    d+00 X
  5.000d-09    0.    d+00 X
  5.500d-09    0.    d+00 X
  6.000d-09    0.    d+00 X
  6.500d-09    0.    d+00 X
  7.000d-09    5.000d+00 +
  7.500d-09    5.000d+00 .
  8.000d-09    5.000d+00 .
  8.500d-09    5.000d+00 .
  9.000d-09    5.000d+00 .
  9.500d-09    5.000d+00 .
  1.000d-08    5.000d+00 .
```



(b) Schematic With Labeled Nodes



(a) Layout With Labeled Nodes

Figure C-6 Transmision Gate SPICE Model

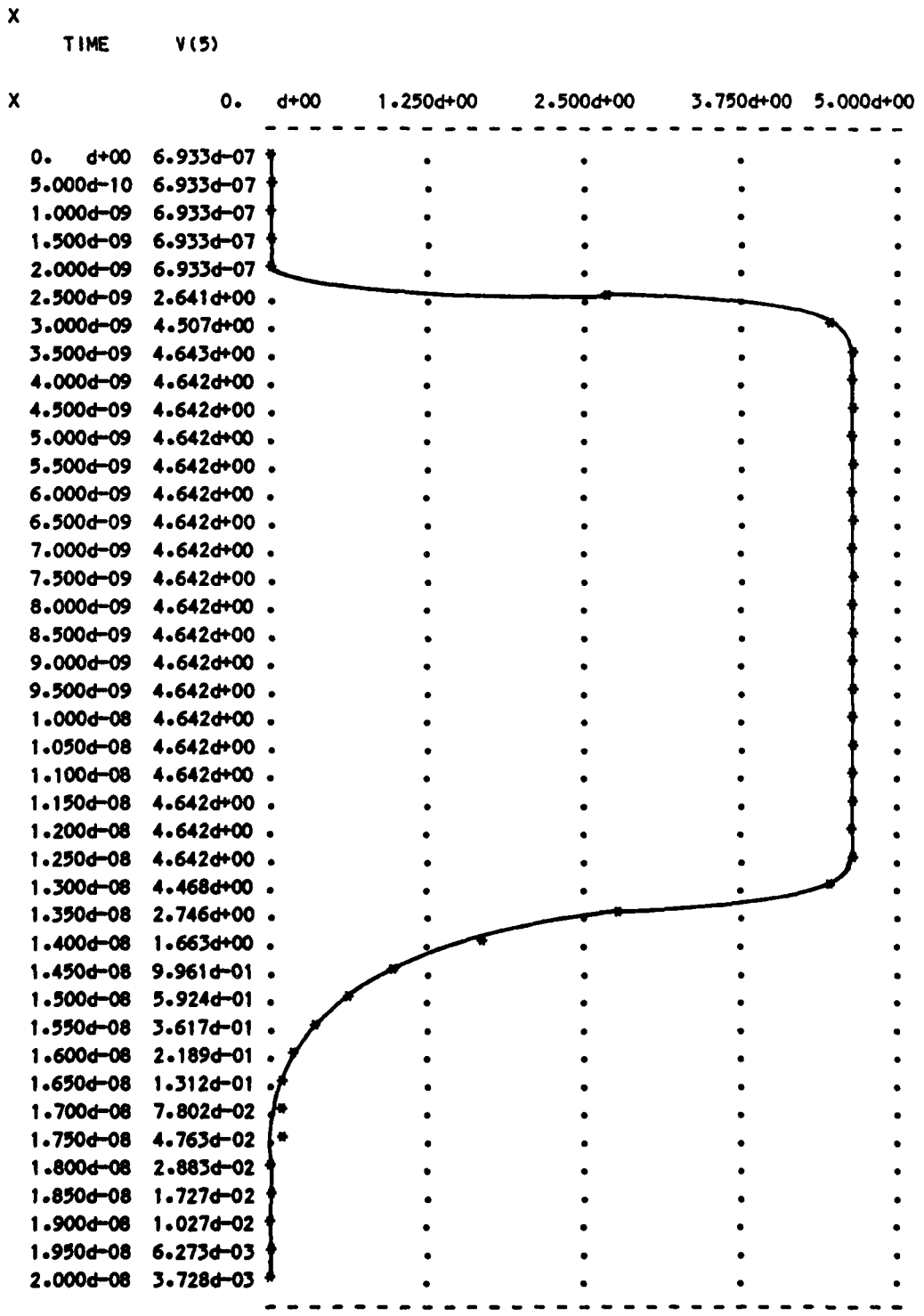
```
1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:37:44******

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=2
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=2
 VDD 3 0 DC 5V
 MPD1 5 1 4 0 N L=4UM W=4UM
 MPU1 5 2 4 3 P L=4UM W=8UM
 CDBK 5 0 0.01PF
 R 5 0 100KOHM
 VIN1 1 0 PULSE (0V 5V 2.0NS 0NS 0NS 10NS)
 VIN2 2 0 PULSE (5V 0V 2.0NS 0NS 0NS 10NS)
 VIN3 4 0 DC 5V
 .TRAN 0.5NS 20.0NS
 .PLOT TRAN V(5) (0V,5V)
 .END
```

Simulates transition to conducting state.

Input B remains constant 5V.

```
1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:37:44******

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************

                 N          P
0TYPE          NMOS       PMOS
0LEVEL          2.000      2.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000

1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:37:44******

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
   NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    0.        (  2)    5.0000    (  3)    5.0000    (  4)    5.0000

(  5)    0.0000

     VOLTAGE SOURCE CURRENTS

     NAME        CURRENT

     VDD       -6.933d-12

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3      -6.933d-12

     TOTAL POWER DISSIPATION   6.93d-11  WATTS

1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:37:44******

0        CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****      OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0             MPD1       MPU1
0MODEL      N          P
 ID         2.68d-19 -1.93d-12
 VGS          -5.000     0.
 VDS          -5.000    -5.000
 VBS          -5.000     0.

1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:37:44******

0        CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****      TRANSIENT ANALYSIS                TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```


X
TIME V(5)
X 0. d+00 1.250d+00 2.500d+00 3.750d+00 5.000d+00
0. d+00 6.933d-07
5.000d-10 6.933d-07
1.000d-09 6.933d-07
1.500d-09 6.933d-07
2.000d-09 6.933d-07
2.500d-09 2.641d+00
3.000d-09 4.507d+00
3.500d-09 4.643d+00
4.000d-09 4.642d+00
4.500d-09 4.642d+00
5.000d-09 4.642d+00
5.500d-09 4.642d+00
6.000d-09 4.642d+00
6.500d-09 4.642d+00
7.000d-09 4.642d+00
7.500d-09 4.642d+00
8.000d-09 4.642d+00
8.500d-09 4.642d+00
9.000d-09 4.642d+00
9.500d-09 4.642d+00
1.000d-08 4.642d+00
1.050d-08 4.642d+00
1.100d-08 4.642d+00
1.150d-08 4.642d+00
1.200d-08 4.642d+00
1.250d-08 4.642d+00
1.300d-08 4.468d+00
1.350d-08 2.746d+00
1.400d-08 1.663d+00
1.450d-08 9.961d-01
1.500d-08 5.924d-01
1.550d-08 3.617d-01
1.600d-08 2.189d-01
1.650d-08 1.312d-01
1.700d-08 7.802d-02
1.750d-08 4.763d-02
1.800d-08 2.883d-02
1.850d-08 1.727d-02
1.900d-08 1.027d-02
1.950d-08 6.273d-03
2.000d-08 3.728d-03

```
1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:38:05*****

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


 .WIDTH OUT=80
 .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
 +LEVEL=2
 .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
 +LEVEL=2
 VDD 3 0 DC 5V
 MPD1 5 1 4 0 N L=4UM W=4UM
 MPU1 5 2 4 3 P L=4UM W=8UM
 CDBK 5 0 0.1PF
 RBK 5 0 100KOHM
 VIN1 1 0 PULSE (5V 0V 2.0NS 0NS 0NS 10NS)
 VIN2 2 0 PULSE (0V 5V 2.0NS 0NS 0NS 10NS)
 VIN3 4 0 DC 5V
 .TRAN 0.5NS 20.0NS
 .PLOT TRAN V(5) (0V,5V)
 .END
```

Simulates transition to non-conducting state.

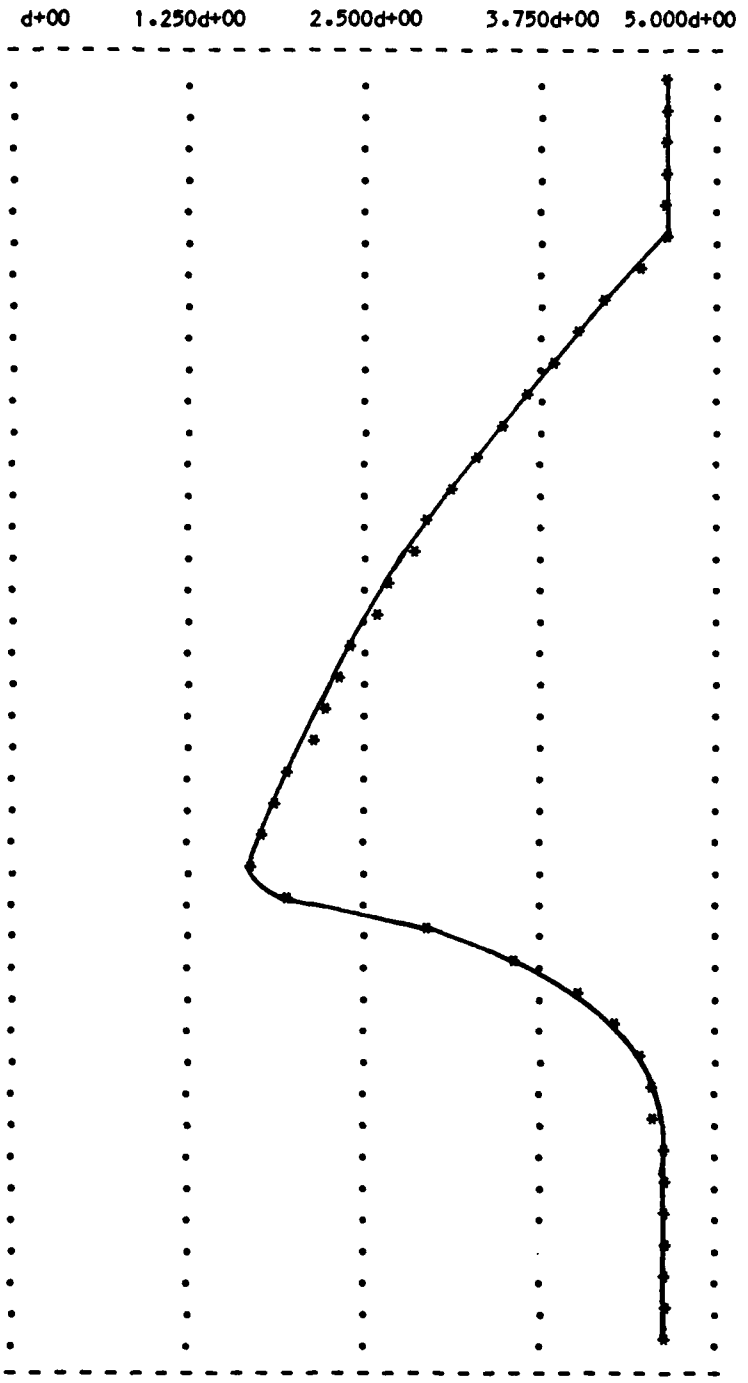
Input B remains constant 5V.

```
1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:38:05*****

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************


                N          P
0TYPE           NMOS       PMOS
0LEVEL            2.000      2.000
0VTO              1.000     -1.000
0KP            1.84d-05   9.21d-06
0GAMMA            1.979      0.685
0PHI              0.743      0.633
0CJ            5.09d-04   1.76d-04
0TOX           7.50d-08   7.50d-08
0NSUB          2.50d+16   3.00d+15
0LD            7.00d-07   7.00d-07
0UO             400.000    200.000

1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:38:05*****

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    0.        (  3)    5.0000    (  4)    5.0000

(  5)    4.6423

     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -4.959d-13

     VIN1      0.   d+00

     VIN2      0.   d+00

     VIN3     -4.642d-05

     TOTAL POWER DISSIPATION   2.32d-04  WATTS

1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:38:05*****

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1       MPU1
OMODEL     N          P
 ID        1.80d-12 -4.64d-05
 VGS         0.       -5.000
 VDS        -0.358    -0.358
 VBS        -5.000     0.

1*******10/21/83 ********  SPICE 2G.1 (15OCT80)  ********15:38:05*****

0       CMOS/SOS TRANSMISSION GATE ANALYSIS (W/L = 2:1)

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

X

TIME	V(5)
0. d+00	4.642d+00
5.000d-10	4.642d+00
1.000d-09	4.642d+00
1.500d-09	4.642d+00
2.000d-09	4.642d+00
2.500d-09	4.671d+00
3.000d-09	4.444d+00
3.500d-09	4.227d+00
4.000d-09	4.021d+00
4.500d-09	3.825d+00
5.000d-09	3.638d+00
5.500d-09	3.461d+00
6.000d-09	3.292d+00
6.500d-09	3.131d+00
7.000d-09	2.979d+00
7.500d-09	2.834d+00
8.000d-09	2.695d+00
8.500d-09	2.564d+00
9.000d-09	2.439d+00
9.500d-09	2.320d+00
1.000d-08	2.206d+00
1.050d-08	2.099d+00
1.100d-08	1.997d+00
1.150d-08	1.899d+00
1.200d-08	1.806d+00
1.250d-08	1.718d+00
1.300d-08	1.980d+00
1.350d-08	2.906d+00
1.400d-08	3.576d+00
1.450d-08	4.029d+00
1.500d-08	4.307d+00
1.550d-08	4.459d+00
1.600d-08	4.541d+00
1.650d-08	4.586d+00
1.700d-08	4.612d+00
1.750d-08	4.625d+00
1.800d-08	4.633d+00
1.850d-08	4.637d+00
1.900d-08	4.639d+00
1.950d-08	4.641d+00
2.000d-08	4.641d+00



Appendix D. CMOS/SOS and NMOS PLA SPICE Analysis

SPICE analysis is presented to verify operation of the CMOS/SOS PLA and also to compare operation to the Stanford NMOS PLA. Circuit diagrams of the two PLA models are included to aid the reader in analyzing the results. Additionally, in order to decrease the possibilities of error while determining circuit nodes, this author used Berkeley's CIFPLOT with the -X option to produce a plot of the CMOS/SOS PLA with automatically numbered nodes. This plot is shown on page D-5 of this appendix.

A 2x3x2 PLA was used, and all four possible input conditions were simulated. The PLA truth table and associated sum-of-product output equations are listed below.

PLA Truth Table

a	a'	b	b'	z1	z2
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	0	0

PLA Output Equations

z1 = a'b

z2 = a'b' + ab'

These four input conditions were simulated using clocked inputs. In all cases, pulse delay was 2ns, pulse duration was 10ns, and transient responses were plotted for a total of 20ns. The order of simulation follows the rows

of the truth table from top to bottom.

The CMOS/SOS PLA simulated almost exactly as predicted. For each input, all truth table values were achieved, thus verifying operation of the PLA. The attached SPICE outputs show all input conditions and resulting transient responses. The only potential problem obvious from these SPICE analyses is a slight asymmetry between pull-up and pull-down responses. This was apparently caused by two NMOS transistors being in series, resulting in an overall increased pull-down delay. Similar problems pertaining to NAND and NOR standard cells were discussed in Chapter 5. NMOS transistor widths may need to be increased to provide a faster pull-down transition. Making NMOS widths equal to PMOS widths (4L) should provide a more symmetrical response, without affecting PLA size.

The NMOS PLA was simulated with inverters on PLA outputs. As the reader may recall, the Stanford NMOS PLA generates inverted outputs and requires external inverters to produce the proper output. Hence, this author considered the inverters to be part of the PLA even though they introduced an additional delay. The NMOS enhancement and depletion models were extracted from Hodges and Jackson [Ref 10:89] and are believed to be applicable. NMOS gate lengths and widths were determined by visual inspection of a NMOS PLA plot and the PLA buffered output (PlaOut) [Ref 4].

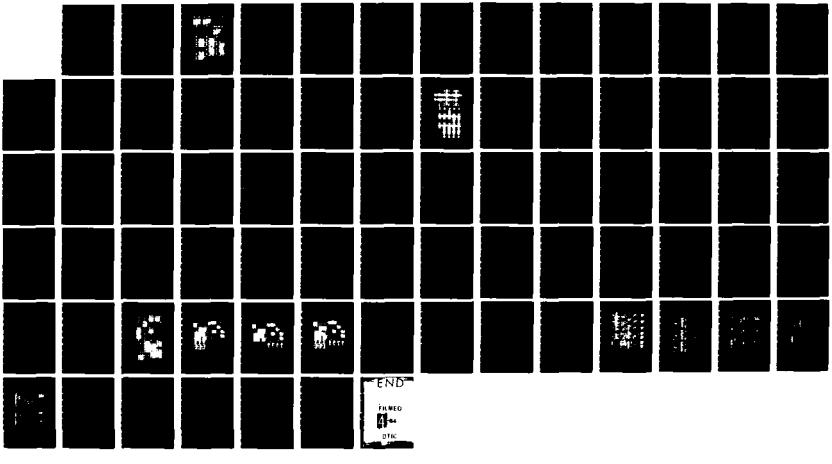
A comparison of the transient responses for both types of PLAs shows that both achieve the correct truth

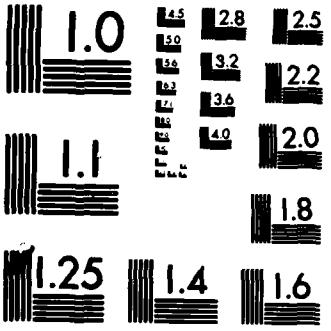
table values. But a significant difference occurs between high-going and low-going transitions. The NMOS PLA exhibits a very gradual pull-up transition to Vdd but a very sharp pull-down to Ground. The CMOS/SOS PLA exhibits a more symmetrical response with only a slightly gradual pull-down response.

The effects of these differences would probably be unnoticeable at normal switching speeds. Considering that the pulse duration for these analyses was 10ns, the equivalent clock rate would be at least 50Mhz. Nevertheless, the CMOS/SOS may tend to have a slightly higher swithing speed limit due to its more symmetrical responses.

A significant difference not related to transient characteristics is the difference in power dissipation. The NMOS PLA dissipates approximately 1.83 milliwatts while the average power dissipation of the CMOS/SOS PLA is about 23.9 picowatts, eight orders of magnitude difference!

AD-A138 310 THE DESIGN AND LAYOUT OF A COMPLEMENTARY METAL OXIDE 3/3
SEMICONDUCTOR SILICO..(U) AIR FORCE INST OF TECH
WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. W E SOMMARS
UNCLASSIFIED DEC 83 AFIT/GE/EE/83D-62 F/G 9/1 NL





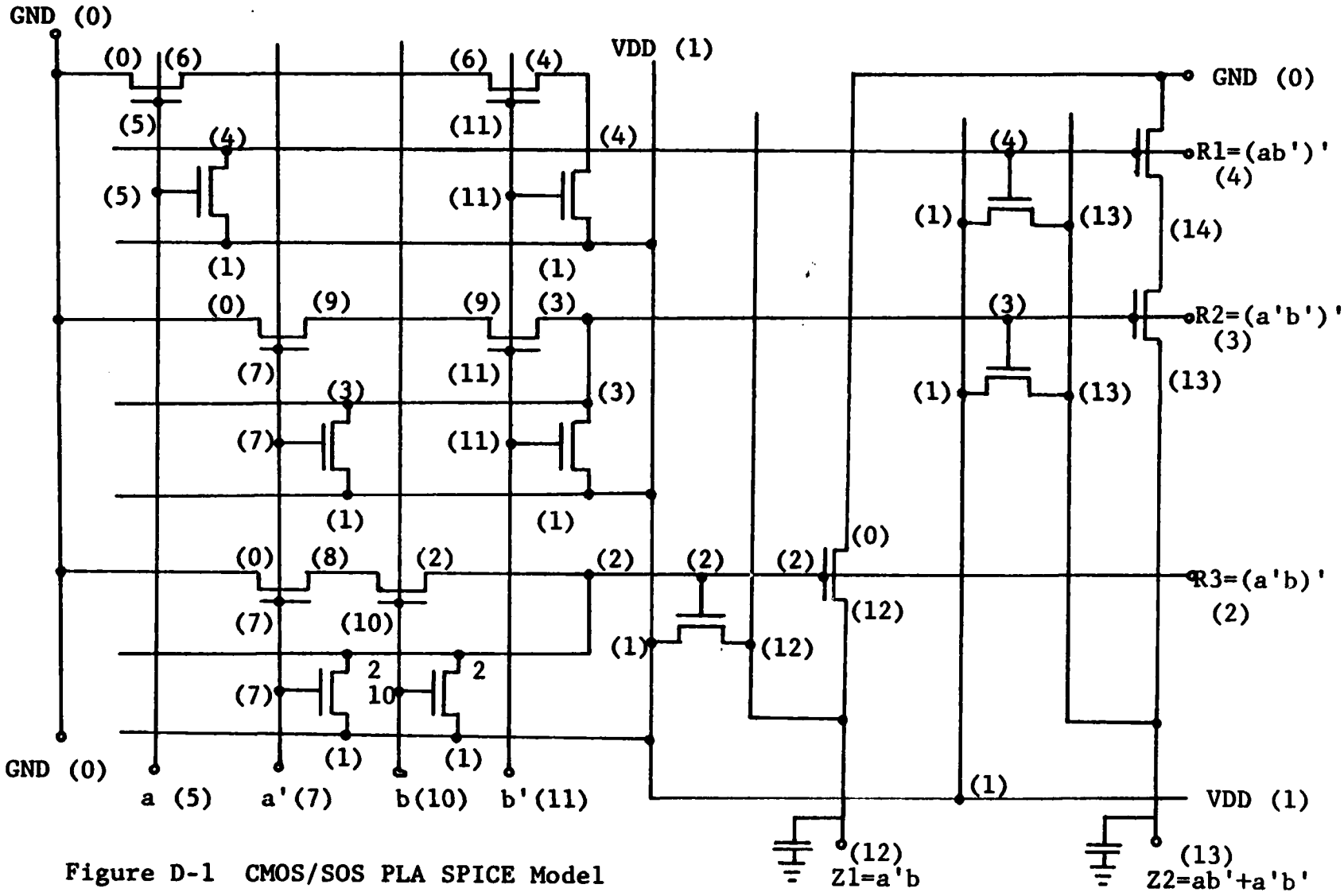


Figure D-1 CMOS/SOS PLA SPICE Model

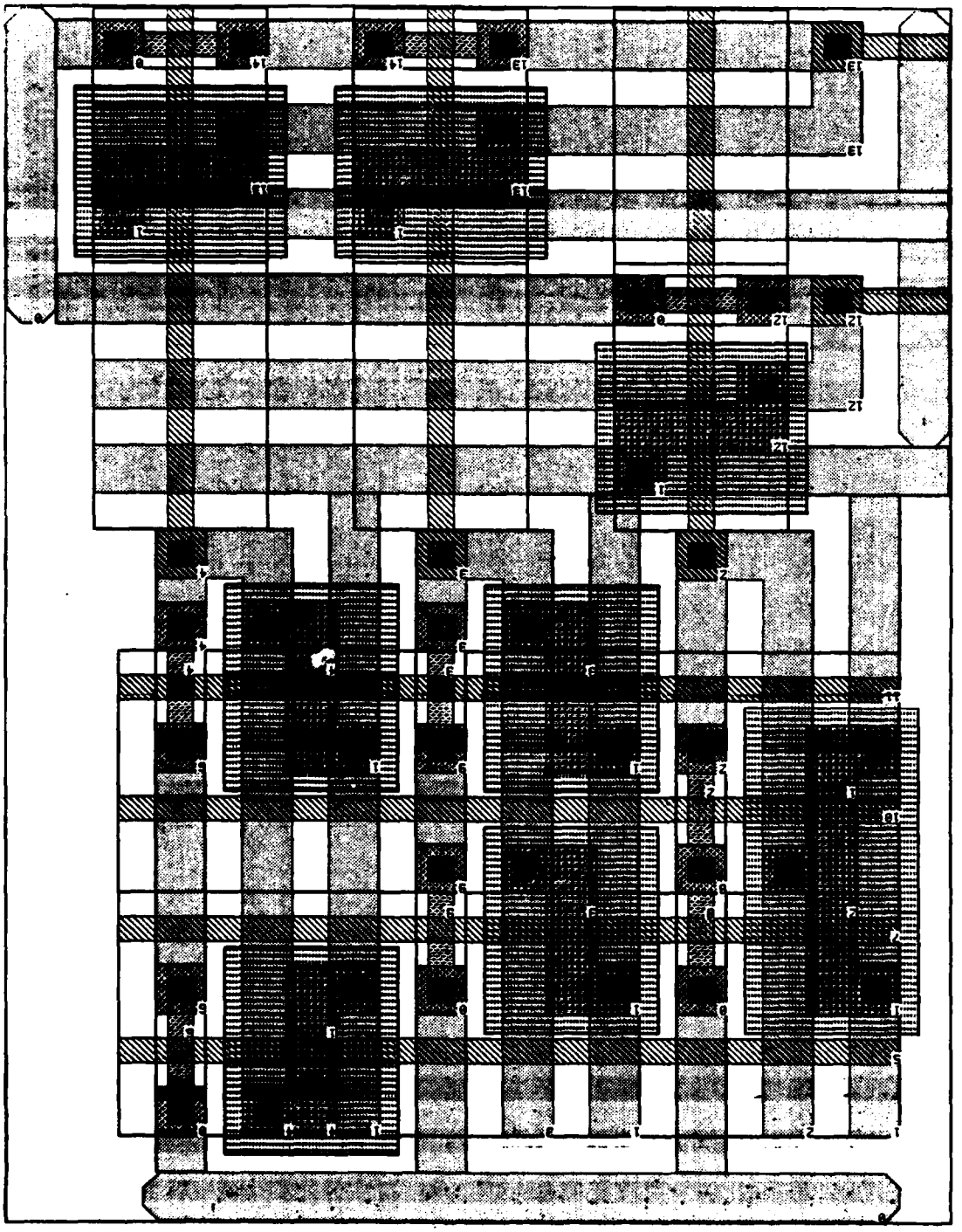


Figure D-2 CMOS/SOS PLA Layout With Labeled Nodes

```
1*******09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:30:47******

0       CMOS/SOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0*****************************************************************************


  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
  +LEVEL=1
  .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 0 5 6 0   N L=4UM W=4UM
  MPU1 1 5 4 1   P L=4UM W=8UM
  MPD2 6 11 4 0  N L=4UM W=4UM
  MPU2 1 11 4 1  P L=4UM W=8UM
  MPD3 0 7 9 0   N L=4UM W=4UM
  MPU3 1 7 3 1   P L=4UM W=8UM
  MPD4 9 11 3 0  N L=4UM W=4UM
  MPU4 1 11 3 1  P L=4UM W=8UM
  MPD5 0 7 8 0   N L=4UM W=4UM
  MPU5 1 7 2 1   P L=4UM W=8UM
  MPD6 8 10 2 0  N L=4UM W=4UM
  MPU6 1 10 2 1  P L=4UM W=8UM
  MPD7 0 2 12 0  N L=4UM W=4UM
  MPU7 1 2 12 1  P L=4UM W=8UM
  MPD8 0 4 14 0  N L=4UM W=4UM
  MPU8 1 4 13 1  P L=4UM W=8UM
  MPD9 14 3 13 0 N L=4UM W=4UM
  MPU9 1 3 13 1  P L=4UM W=8UM
  CDBK1 12 0 0.1PF
  CDBK2 13 0 0.1PF
  VIN1 5  0 PULSE (5V 0V 2NS ONS ONS 10NS)
  VIN2 7  0 PULSE (0V 5V 2NS ONS ONS 10NS)
  VIN3 10 0 PULSE (5V 0V 2NS ONS ONS 10NS)
  VIN4 11 0 PULSE (0V 5V 2NS ONS ONS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(12) V(13) (0V,5V)
  .END
1*******09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:30:47******

0       CMOS/SOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

Simulates first row of truth table.

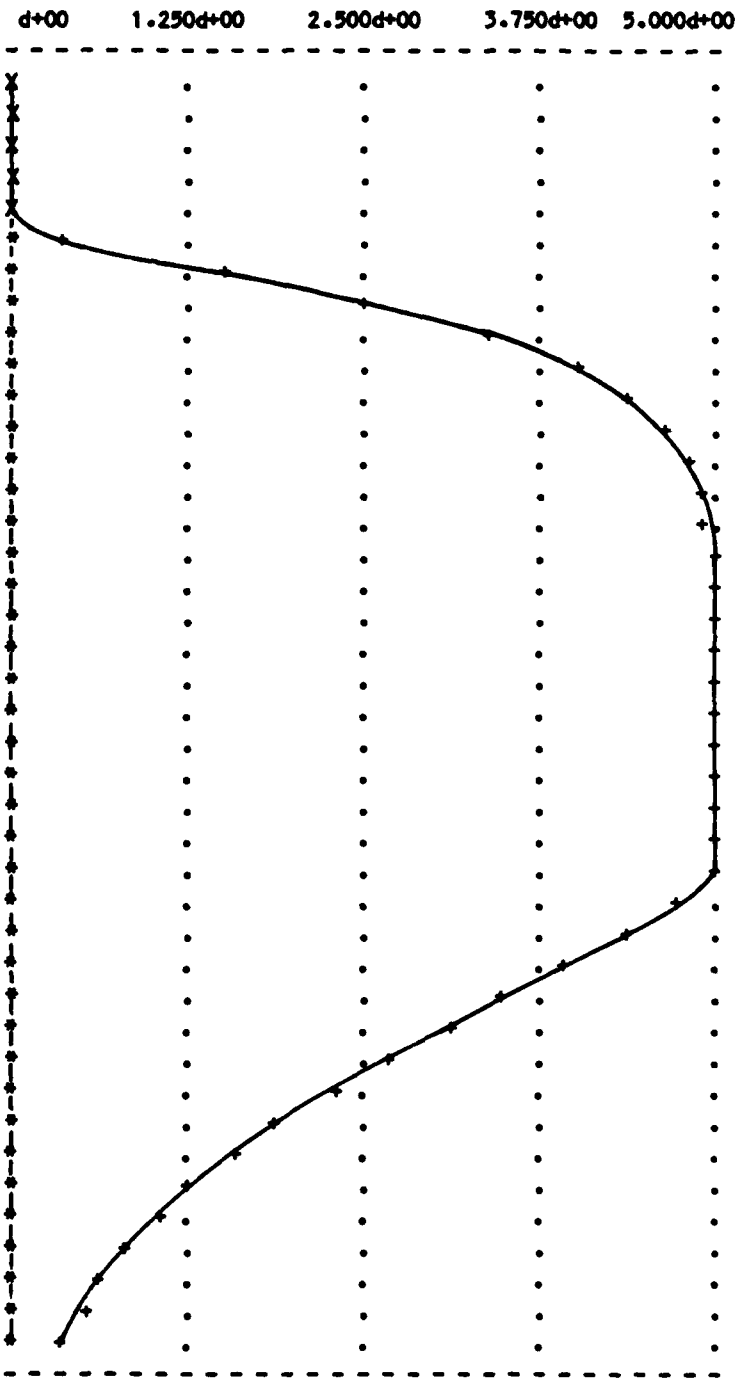
```
                N          P
0TYPE           NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000


1*******09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:30:47******

0       CMOS/SOS PLA ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    5.0000    (  4)    5.0000

(  5)    5.0000    (  6)    0.        (  7)    0.        (  8)    2.2702

(  9)    0.        ( 10)    5.0000    ( 11)    0.        ( 12)    0.0000

( 13)    0.0000    ( 14)    0.0000


    VOLTAGE SOURCE CURRENTS

    NAME         CURRENT

    VDD       -4.789d-11

    VIN1       0.   d+00

    VIN2       0.   d+00

    VIN3       0.   d+00

    VIN4       0.   d+00
```

```
     TOTAL POWER DISSIPATION   2.39d-10  WATTS

1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:30:47******

0       CMOS/SOS PLA ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1       MPU1       MPD2       MPU2       MPD3       MPU3       MPD4
0MODEL       N          P          N          P          N          P          N
 ID          0.  d+00   0.  d+00   0.  d+00   6.93d-12   0.  d+00   3.47d-12   0.  d+00
 VGS           5.000      0.000     -5.000     -5.000      0.        -5.000     -5.000
 VDS           0.         0.000     -5.000      0.000      0.         0.000     -5.000
 VBS           0.         0.000     -5.000      0.000      0.         0.000     -5.000


0            MPU4       MPD5       MPU5       MPD6       MPU6       MPD7       MPU7
0MODEL       P          N          P          N          P          N          P
 ID          3.47d-12   0.  d+00   1.29d-11  -6.31d-12   0.  d+00  -6.93d-12   0.  d+00
 VGS          -5.000     -2.270     -5.000      0.000      0.000      5.000      5.000
 VDS           0.000     -2.270      0.000     -2.730      0.000     -0.000      5.000
 VBS           0.000     -2.270      0.000     -5.000      0.000     -0.000      5.000


0            MPD8       MPU8       MPD9       MPU9
0MODEL       N          P          N          P
 ID         -1.36d-11   0.  d+00  -1.39d-11   0.  d+00
 VGS           5.000      5.000      5.000      5.000
 VDS          -0.000      5.000     -0.000      5.000
 VBS          -0.000      5.000     -0.000      5.000



1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:30:47******

0       CMOS/SOS PLA ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

*: V(12)
+: V(13)
X

TIME	V(12)
0. d+00	6.117d-08
5.000d-10	6.117d-08
1.000d-09	6.117d-08
1.500d-09	6.117d-08
2.000d-09	6.117d-08
2.500d-09	6.137d-08
3.000d-09	6.129d-08
3.500d-09	6.124d-08
4.000d-09	6.121d-08
4.500d-09	6.119d-08
5.000d-09	6.119d-08
5.500d-09	6.118d-08
6.000d-09	6.118d-08
6.500d-09	6.118d-08
7.000d-09	6.118d-08
7.500d-09	6.118d-08
8.000d-09	6.118d-08
8.500d-09	6.117d-08
9.000d-09	6.117d-08
9.500d-09	6.117d-08
1.000d-08	6.117d-08
1.050d-08	6.117d-08
1.100d-08	6.117d-08
1.150d-08	6.117d-08
1.200d-08	6.117d-08
1.250d-08	6.117d-08
1.300d-08	6.145d-08
1.350d-08	6.133d-08
1.400d-08	6.126d-08
1.450d-08	6.122d-08
1.500d-08	6.120d-08
1.550d-08	6.119d-08
1.600d-08	6.118d-08
1.650d-08	6.118d-08
1.700d-08	6.118d-08
1.750d-08	6.118d-08
1.800d-08	6.118d-08
1.850d-08	6.118d-08
1.900d-08	6.118d-08
1.950d-08	6.117d-08
2.000d-08	6.117d-08



```
1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:25:28******

0       CMOS/SOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0*****************************************************************************


  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
  +LEVEL=1
  .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 0 5 6 0   N L=4UM W=4UM
  MPU1 1 5 4 1   P L=4UM W=8UM
  MPD2 6 11 4 0  N L=4UM W=4UM
  MPU2 1 11 4 1  P L=4UM W=8UM
  MPD3 0 7 9 0   N L=4UM W=4UM
  MPU3 1 7 3 1   P L=4UM W=8UM
  MPD4 9 11 3 0  N L=4UM W=4UM
  MPU4 1 11 3 1  P L=4UM W=8UM
  MPD5 0 7 8 0   N L=4UM W=4UM
  MPU5 1 7 2 1   P L=4UM W=8UM
  MPD6 8 10 2 0  N L=4UM W=4UM
  MPU6 1 10 2 1  P L=4UM W=8UM
  MPD7 0 2 12 0  N L=4UM W=4UM
  MPU7 1 2 12 1  P L=4UM W=8UM
  MPD8 0 4 14 0  N L=4UM W=4UM
  MPU8 1 4 13 1  P L=4UM W=8UM
  MPD9 14 3 13 0 N L=4UM W=4UM
  MPU9 1 3 13 1  P L=4UM W=8UM
  CDBK1 12 0 0.1PF
  CDBK2 13 0 0.1PF
  VIN1 5  0 PULSE (5V 0V 2NS ONS ONS 10NS)
  VIN2 7  0 PULSE (0V 5V 2NS ONS ONS 10NS)
  VIN3 10 0 PULSE (0V 5V 2NS ONS ONS 10NS)
  VIN4 11 0 PULSE (5V 0V 2NS ONS ONS 10NS)
  .TRAN 0.5NS 17NS
  .PLOT TRAN V(12) V(13) (0V,5V)
  .END
1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:25:28******

0       CMOS/SOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

Simulates second row of truth table.

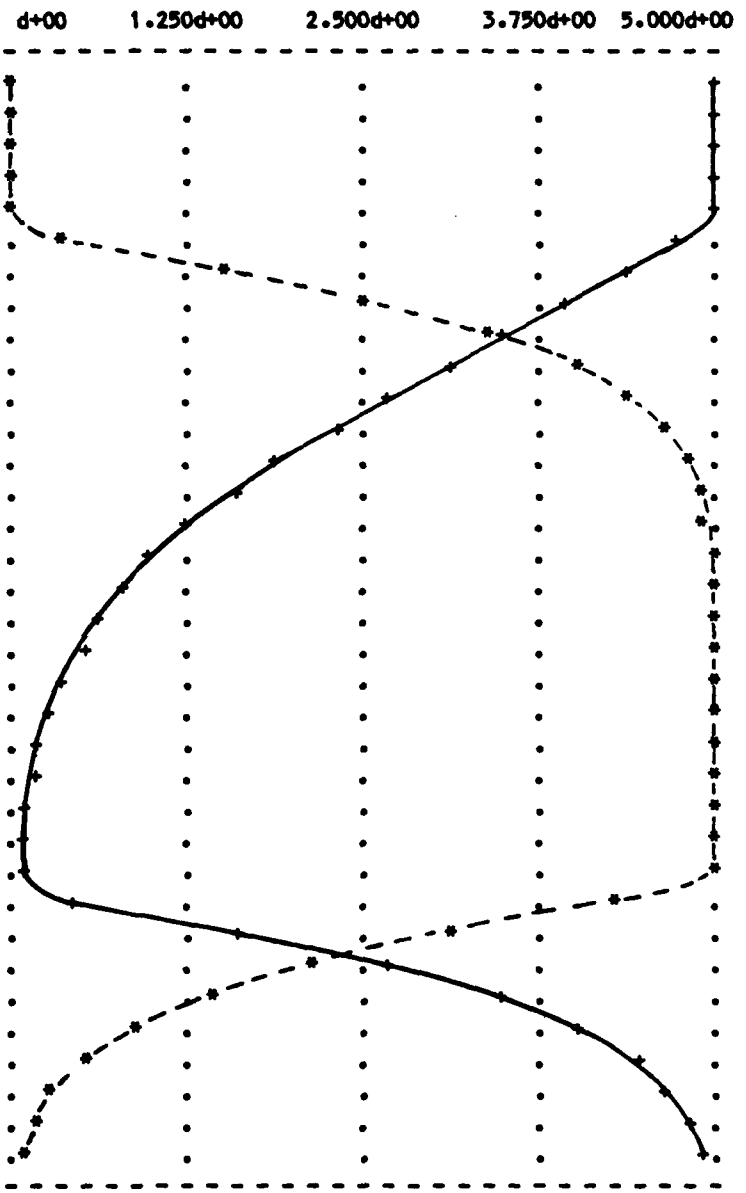
```
                N          P
OTYPE           NMOS       PMOS
OLEVEL          1.000      1.000
OVTO            1.000      -1.000
OKP             1.84d-05   9.21d-06
OGAMMA          1.979      0.685
OPHI            0.743      0.633
OCJ             5.09d-04   1.76d-04
OTOX            7.50d-08   7.50d-08
ONSUB           2.50d+16   3.00d+15
OLD             7.00d-07   7.00d-07
OUO             400.000    200.000


1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:25:28******

0       CMOS/SOS PLA ANALYSIS

0*****      INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0**********************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    5.0000    (  4)    0.0000

(  5)    5.0000    (  6)    0.0000    (  7)    0.        (  8)    0.

(  9)    2.2702    ( 10)    0.        ( 11)    5.0000    ( 12)    0.0000

( 13)    5.0000    ( 14)    2.2702


     VOLTAGE SOURCE CURRENTS

     NAME       CURRENT

     VDD      -5.419d-11

     VIN1      0.   d+00

     VIN2      0.   d+00

     VIN3      0.   d+00

     VIN4      0.   d+00
```

```
     TOTAL POWER DISSIPATION   2.71d-10  WATTS

1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:25:28******

0       CMOS/SOS PLA ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS


0            MPD1       MPU1       MPD2       MPU2       MPD3       MPU3       MPD4
0MODEL     N          P          N          P          N          P          N
 ID       -1.39d-11  0.  d+00  -1.39d-11  0.  d+00  0.  d+00  1.29d-11  -6.31d-12
 VGS        5.000      5.000      5.000      5.000     -2.270     -5.000      0.000
 VDS       -0.000      5.000     -0.000      5.000     -2.270      0.000     -2.730
 VBS       -0.000      5.000     -0.000      5.000     -2.270      0.000     -5.000


0            MPU4       MPD5       MPU5       MPD6       MPU6       MPD7       MPU7
0MODEL     P          N          P          N          P          N          P
 ID       0.  d+00  0.  d+00  3.47d-12  0.  d+00  3.47d-12  -6.93d-12  0.  d+00
 VGS        0.000      0.        -5.000     -5.000     -5.000      5.000      5.000
 VDS        0.000      0.         0.000     -5.000      0.000     -0.000      5.000
 VBS        0.000      0.         0.000     -5.000      0.000     -0.000      5.000


0            MPD8       MPU8       MPD9       MPU9
0MODEL     N          P          N          P
 ID       0.  d+00  1.32d-11  -7.66d-12  0.  d+00
 VGS       -2.270     -5.000     -0.000     -0.000
 VDS       -2.270      0.000     -2.730      0.000
 VBS       -2.270      0.000     -5.000      0.000



1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:25:28******

0       CMOS/SOS PLA ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

OLEGEND:

*: V(12)
+: V(13)
X

TIME	V(12)
0. d+00	6.117d-08
5.000d-10	6.117d-08
1.000d-09	6.117d-08
1.500d-09	6.117d-08
2.000d-09	6.117d-08
2.500d-09	3.524d-01
3.000d-09	1.481d+00
3.500d-09	2.518d+00
4.000d-09	3.377d+00
4.500d-09	3.983d+00
5.000d-09	4.394d+00
5.500d-09	4.644d+00
6.000d-09	4.796d+00
6.500d-09	4.883d+00
7.000d-09	4.934d+00
7.500d-09	4.963d+00
8.000d-09	4.979d+00
8.500d-09	4.988d+00
9.000d-09	4.993d+00
9.500d-09	4.996d+00
1.000d-08	4.998d+00
1.050d-08	4.999d+00
1.100d-08	4.999d+00
1.150d-08	5.000d+00
1.200d-08	5.000d+00
1.250d-08	5.000d+00
1.300d-08	4.275d+00
1.350d-08	3.162d+00
1.400d-08	2.162d+00
1.450d-08	1.389d+00
1.500d-08	8.609d-01
1.550d-08	5.047d-01
1.600d-08	2.971d-01
1.650d-08	1.686d-01
1.700d-08	9.541d-02



```
1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:32:08******

0       CMOS/SOS PLA ANALYSIS

0****     INPUT LISTING                        TEMPERATURE =   27.000 DEG C

0*****************************************************************************



  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
  +LEVEL=1
  .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 0 5 6 0   N L=4UM W=4UM
  MPU1 1 5 4 1   P L=4UM W=8UM
  MPD2 6 11 4 0  N L=4UM W=4UM
  MPU2 1 11 4 1  P L=4UM W=8UM
  MPD3 0 7 9 0   N L=4UM W=4UM
  MPU3 1 7 3 1   P L=4UM W=8UM
  MPD4 9 11 3 0  N L=4UM W=4UM
  MPU4 1 11 3 1  P L=4UM W=8UM
  MPD5 0 7 8 0   N L=4UM W=4UM
  MPU5 1 7 2 1   P L=4UM W=8UM
  MPD6 8 10 2 0  N L=4UM W=4UM
  MPU6 1 10 2 1  P L=4UM W=8UM
  MPD7 0 2 12 0  N L=4UM W=4UM
  MPU7 1 2 12 1  P L=4UM W=8UM
  MPD8 0 4 14 0  N L=4UM W=4UM
  MPU8 1 4 13 1  P L=4UM W=8UM
  MPD9 14 3 13 0 N L=4UM W=4UM
  MPU9 1 3 13 1  P L=4UM W=8UM
  CDBK1 12 0 0.1PF
  CDBK2 13 0 0.1PF
  VIN1 5  0 PULSE (0V 5V 2NS 0NS 0NS 10NS)    Simulates third row
  VIN2 7  0 PULSE (5V 0V 2NS 0NS 0NS 10NS)    of truth table.
  VIN3 10 0 PULSE (5V 0V 2NS 0NS 0NS 10NS)
  VIN4 11 0 PULSE (0V 5V 2NS 0NS 0NS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(12) V(13) (0V,5V)
  .END
1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:32:08******

0       CMOS/SOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS              TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

	N	P
OTYPE	NMOS	PMOS
OLEVEL	1.000	1.000
OVTO	1.000	-1.000
OKP	1.84d-05	9.21d-06
OGAMMA	1.979	0.685
OPHI	0.743	0.633
OCJ	5.09d-04	1.76d-04
OTOX	7.50d-08	7.50d-08
ONSUB	2.50d+16	3.00d+15
OLD	7.00d-07	7.00d-07
OUO	400.000	200.000

1*******09/21/83 ******** SPICE 2G.1 (15OCT80) ********22:32:08******

0 CMOS/SOS PLA ANALYSIS

0**** INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

0**********

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	5.0000	(2)	0.0000	(3)	5.0000	(4)	5.0000
(5)	0.	(6)	0.	(7)	5.0000	(8)	0.0000
(9)	0.	(10)	5.0000	(11)	0.	(12)	5.0000
(13)	0.0000	(14)	0.0000				

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
VDD	-4.853d-11
VIN1	0. d+00
VIN2	0. d+00
VIN3	0. d+00
VIN4	0. d+00

TOTAL POWER DISSIPATION 2.43d-10 WATTS

1********09/21/83 ******** SPICE 2G.1 (15OCT80) ********22:32:08******

0 CMOS/SOS PLA ANALYSIS

0**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

0**********

0

0**** MOSFETS

0	MPD1	MPU1	MPD2	MPU2	MPD3	MPU3	MPD4
OMODEL	N	P	N	P	N	P	N
ID	0. d+00	3.47d-12	0. d+00	3.47d-12	0. d+00	0. d+00	0. d+00
VGS	0.	-5.000	-5.000	-5.000	5.000	0.000	-5.000
VDS	0.	0.000	-5.000	0.000	0.	0.000	-5.000
VBS	0.	0.000	-5.000	0.000	0.	0.000	-5.000

0	MPU4	MPD5	MPU5	MPD6	MPU6	MPD7	MPU7
OMODEL	P	N	P	N	P	N	P
ID	6.93d-12	-1.39d-11	0. d+00	-1.39d-11	0. d+00	0. d+00	6.93d-12
VGS	-5.000	5.000	5.000	5.000	5.000	-5.000	-5.000
VDS	0.000	-0.000	5.000	-0.000	5.000	-5.000	0.000
VBS	0.000	-0.000	5.000	-0.000	5.000	-5.000	0.000

0	MPD8	MPU8	MPD9	MPU9
OMODEL	N	P	N	P
ID	-1.36d-11	0. d+00	-1.39d-11	0. d+00
VGS	5.000	5.000	5.000	5.000
VDS	-0.000	5.000	-0.000	5.000
VBS	-0.000	5.000	-0.000	5.000

1********09/21/83 ******** SPICE 2G.1 (15OCT80) ********22:32:08******

0 CMOS/SOS PLA ANALYSIS

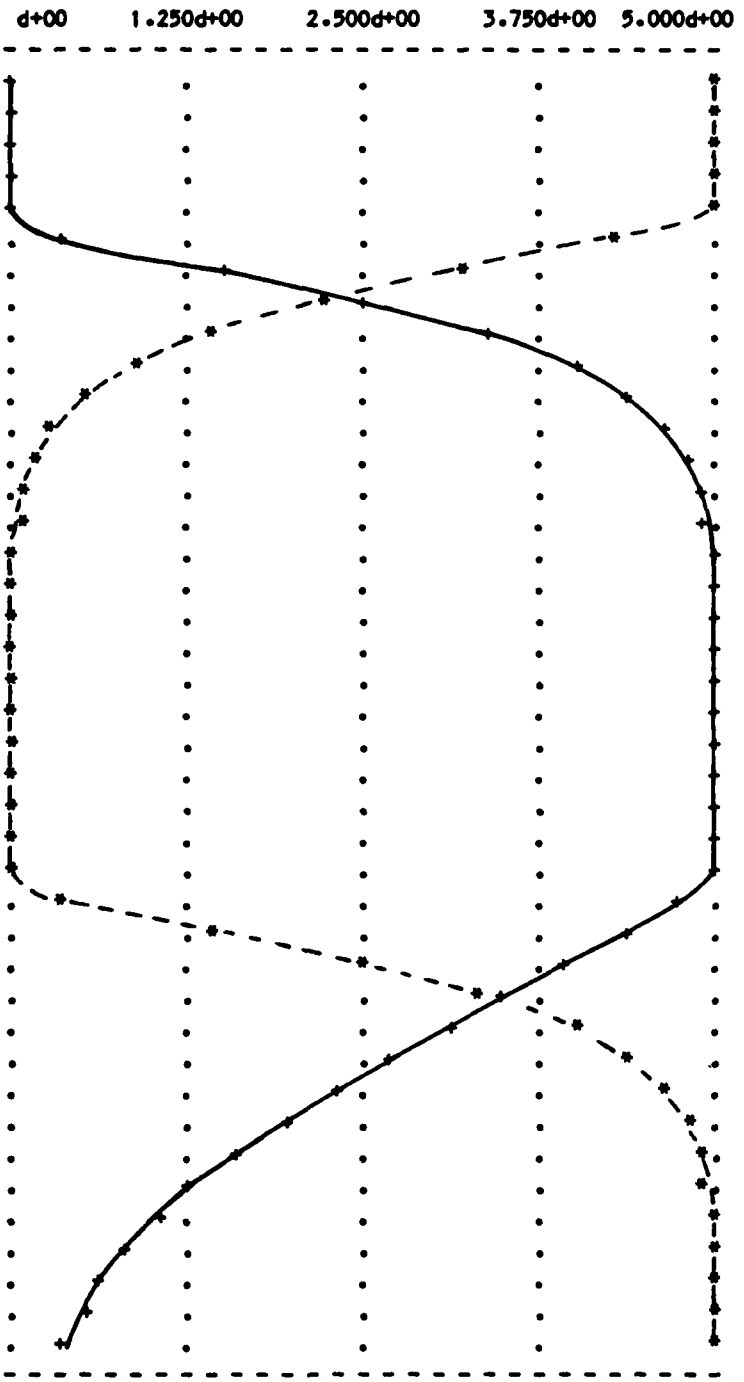
0**** TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

0**********

OLEGEND:

*: V(12)
+: V(13)
X

TIME	V(12)
0. d+00	5.000d+00
5.000d-10	5.000d+00
1.000d-09	5.000d+00
1.500d-09	5.000d+00
2.000d-09	5.000d+00
2.500d-09	4.329d+00
3.000d-09	3.217d+00
3.500d-09	2.208d+00
4.000d-09	1.440d+00
4.500d-09	8.803d-01
5.000d-09	5.200d-01
5.500d-09	3.056d-01
6.000d-09	1.755d-01
6.500d-09	9.869d-02
7.000d-09	5.538d-02
7.500d-09	3.166d-02
8.000d-09	1.788d-02
8.500d-09	9.947d-03
9.000d-09	5.550d-03
9.500d-09	3.165d-03
1.000d-08	1.784d-03
1.050d-08	9.917d-04
1.100d-08	5.531d-04
1.150d-08	3.153d-04
1.200d-08	1.778d-04
1.250d-08	9.750d-05
1.300d-08	3.272d-01
1.350d-08	1.453d+00
1.400d-08	2.491d+00
1.450d-08	3.345d+00
1.500d-08	3.976d+00
1.550d-08	4.386d+00
1.600d-08	4.638d+00
1.650d-08	4.792d+00
1.700d-08	4.883d+00
1.750d-08	4.934d+00
1.800d-08	4.962d+00
1.850d-08	4.979d+00
1.900d-08	4.988d+00
1.950d-08	4.993d+00
2.000d-08	4.996d+00



```
1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:32:51******

0       CMOS/SOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0*****************************************************************************


  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL N NMOS (VTO=1V TOX=75NM UO=400 NSUB=2.5E16 LD=0.7UM)
  +LEVEL=1
  .MODEL P PMOS (VTO=-1V TOX=75NM UO=200 NSUB=3E15 LD=0.7UM)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 0 5 6 0   N L=4UM W=4UM
  MPU1 1 5 4 1   P L=4UM W=8UM
  MPD2 6 11 4 0  N L=4UM W=4UM
  MPU2 1 11 4 1  P L=4UM W=8UM
  MPD3 0 7 9 0   N L=4UM W=4UM
  MPU3 1 7 3 1   P L=4UM W=8UM
  MPD4 9 11 3 0  N L=4UM W=4UM
  MPU4 1 11 3 1  P L=4UM W=8UM
  MPD5 0 7 8 0   N L=4UM W=4UM
  MPU5 1 7 2 1   P L=4UM W=8UM
  MPD6 8 10 2 0  N L=4UM W=4UM
  MPU6 1 10 2 1  P L=4UM W=8UM
  MPD7 0 2 12 0  N L=4UM W=4UM
  MPU7 1 2 12 1  P L=4UM W=8UM
  MPD8 0 4 14 0  N L=4UM W=4UM
  MPU8 1 4 13 1  P L=4UM W=8UM
  MPD9 14 3 13 0 N L=4UM W=4UM
  MPU9 1 3 13 1  P L=4UM W=8UM
  CDBK1 12 0 0.1PF
  CDBK2 13 0 0.1PF
  VIN1 5  0 PULSE (0V 5V 2NS 0NS 0NS 10NS)    Simulates last row
  VIN2 7  0 PULSE (5V 0V 2NS 0NS 0NS 10NS)    of truth table.
  VIN3 10 0 PULSE (0V 5V 2NS 0NS 0NS 10NS)
  VIN4 11 0 PULSE (5V 0V 2NS 0NS 0NS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(12) V(13) (0V,5V)
  .END
1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:32:51******

0       CMOS/SOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```

```
                N          P
0TYPE          NMOS       PMOS
0LEVEL          1.000      1.000
0VTO            1.000     -1.000
0KP          1.84d-05   9.21d-06
0GAMMA          1.979      0.685
0PHI            0.743      0.633
0CJ          5.09d-04   1.76d-04
0TOX         7.50d-08   7.50d-08
0NSUB        2.50d+16   3.00d+15
0LD          7.00d-07   7.00d-07
0UO           400.000    200.000


1********09/21/83 ********  SPICE 2G.1 (15OCT80)  ********22:32:51******

0        CMOS/SOS PLA ANALYSIS

0*****      INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0**********************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    0.0000    (  4)    5.0000

(  5)    0.        (  6)    2.2702    (  7)    5.0000    (  8)    0.

(  9)    0.0000    ( 10)    0.        ( 11)    5.0000    ( 12)    0.0000

( 13)    5.0000    ( 14)   -0.0000


     VOLTAGE SOURCE CURRENTS

     NAME         CURRENT

     VDD       -4.789d-11

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3       0.   d+00

     VIN4       0.   d+00
```

TOTAL POWER DISSIPATION 2.39d-10 WATTS

1********09/21/83 ******** SPICE 2G.1 (15OCT80) ********22:32:51*****

0 CMOS/SOS PLA ANALYSIS

0**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

0**********

0

0**** MOSFETS

0	MPD1	MPU1	MPD2	MPU2	MPD3	MPU3	MPD4
OMODEL	N	P	N	P	N	P	N
ID	0. d+00	1.29d-11	-6.31d-12	0. d+00	-1.39d-11	0. d+00	-1.39d-11
VGS	-2.270	-5.000	0.000	0.000	5.000	5.000	5.000
VDS	-2.270	0.000	-2.730	0.000	-0.000	5.000	-0.000
VBS	-2.270	0.000	-5.000	0.000	-0.000	5.000	-0.000

0	MPU4	MPD5	MPU5	MPD6	MPU6	MPD7	MPU7
OMODEL	P	N	P	N	P	N	P
ID	0. d+00	0. d+00	0. d+00	0. d+00	6.93d-12	-6.93d-12	0. d+00
VGS	5.000	5.000	0.000	-5.000	-5.000	5.000	5.000
VDS	5.000	0.	0.000	-5.000	0.000	-0.000	5.000
VBS	5.000	0.	0.000	-5.000	0.000	-0.000	5.000

0	MPD8	MPU8	MPD9	MPU9
OMODEL	N	P	N	P
ID	3.65d-19	0. d+00	1.39d-31	6.93d-12
VGS	5.000	-0.000	-5.000	-5.000
VDS	0.000	0.000	-5.000	0.000
VBS	0.000	0.000	-5.000	0.000

1********09/21/83 ******** SPICE 2G.1 (15OCT80) ********22:32:51*****

0 CMOS/SOS PLA ANALYSIS

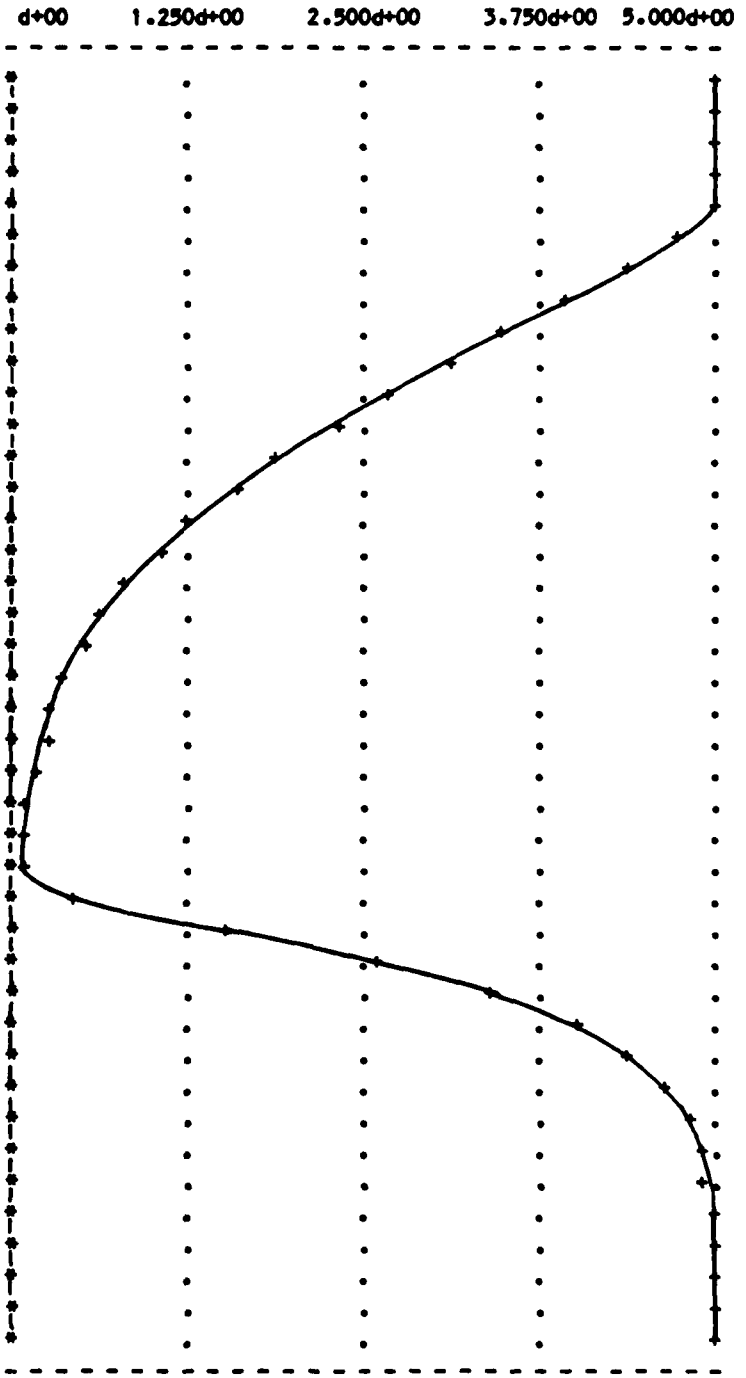
0**** TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

0**********

OLEGEND:

*: V(12)
+: V(13)
X

TIME	V(12)
0. d+00	6.117d-08
5.000d-10	6.117d-08
1.000d-09	6.117d-08
1.500d-09	6.117d-08
2.000d-09	6.117d-08
2.500d-09	6.145d-08
3.000d-09	6.133d-08
3.500d-09	6.126d-08
4.000d-09	6.122d-08
4.500d-09	6.120d-08
5.000d-09	6.119d-08
5.500d-09	6.118d-08
6.000d-09	6.118d-08
6.500d-09	6.118d-08
7.000d-09	6.118d-08
7.500d-09	6.118d-08
8.000d-09	6.118d-08
8.500d-09	6.118d-08
9.000d-09	6.117d-08
9.500d-09	6.117d-08
1.000d-08	6.117d-08
1.050d-08	6.117d-08
1.100d-08	6.117d-08
1.150d-08	6.117d-08
1.200d-08	6.117d-08
1.250d-08	6.117d-08
1.300d-08	6.137d-08
1.350d-08	6.129d-08
1.400d-08	6.124d-08
1.450d-08	6.121d-08
1.500d-08	6.119d-08
1.550d-08	6.119d-08
1.600d-08	6.118d-08
1.650d-08	6.118d-08
1.700d-08	6.118d-08
1.750d-08	6.118d-08
1.800d-08	6.118d-08
1.850d-08	6.118d-08
1.900d-08	6.117d-08
1.950d-08	6.117d-08
2.000d-08	6.117d-08



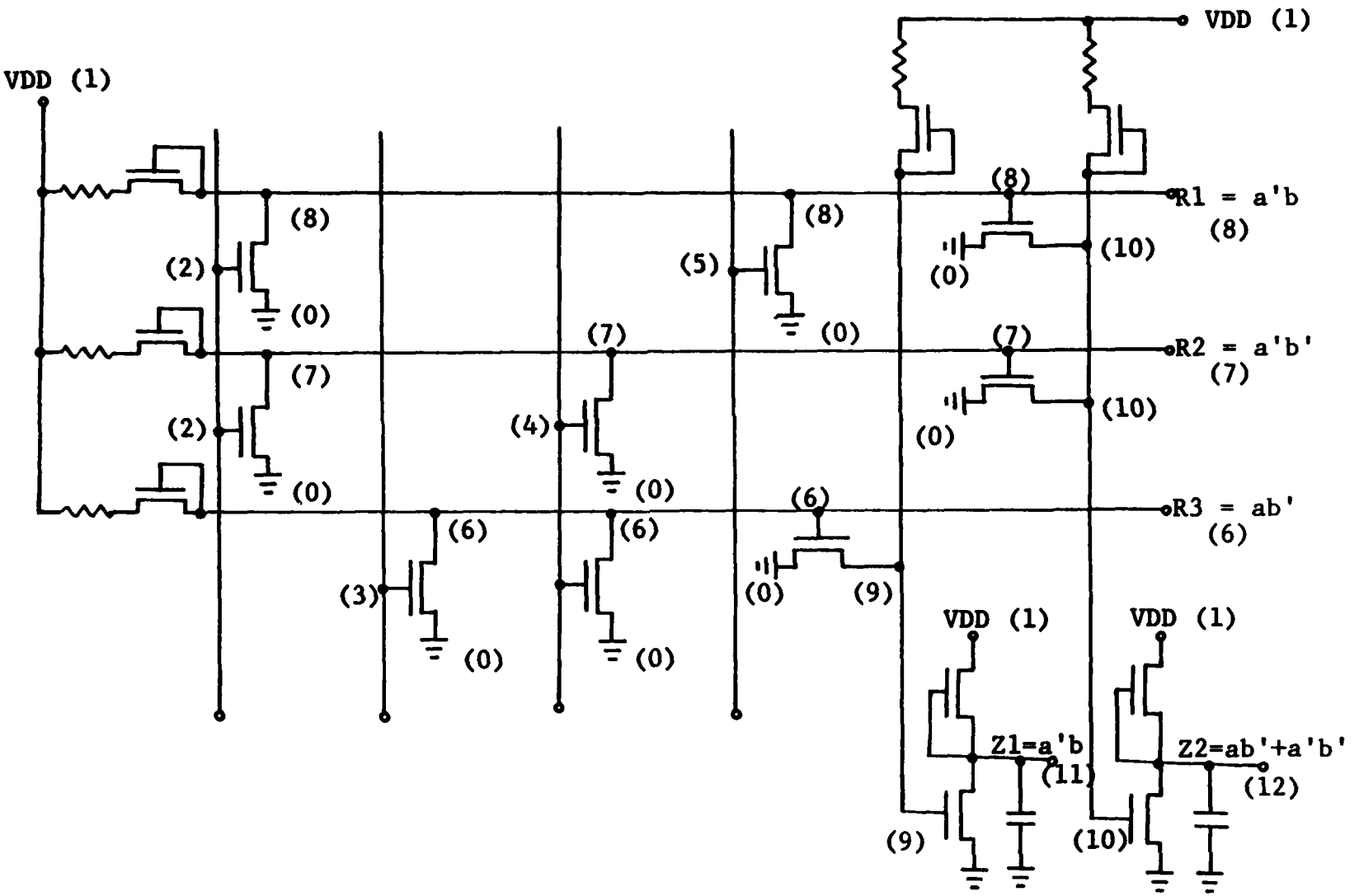


Figure D-3 NMOS PLA SPICE MOdel

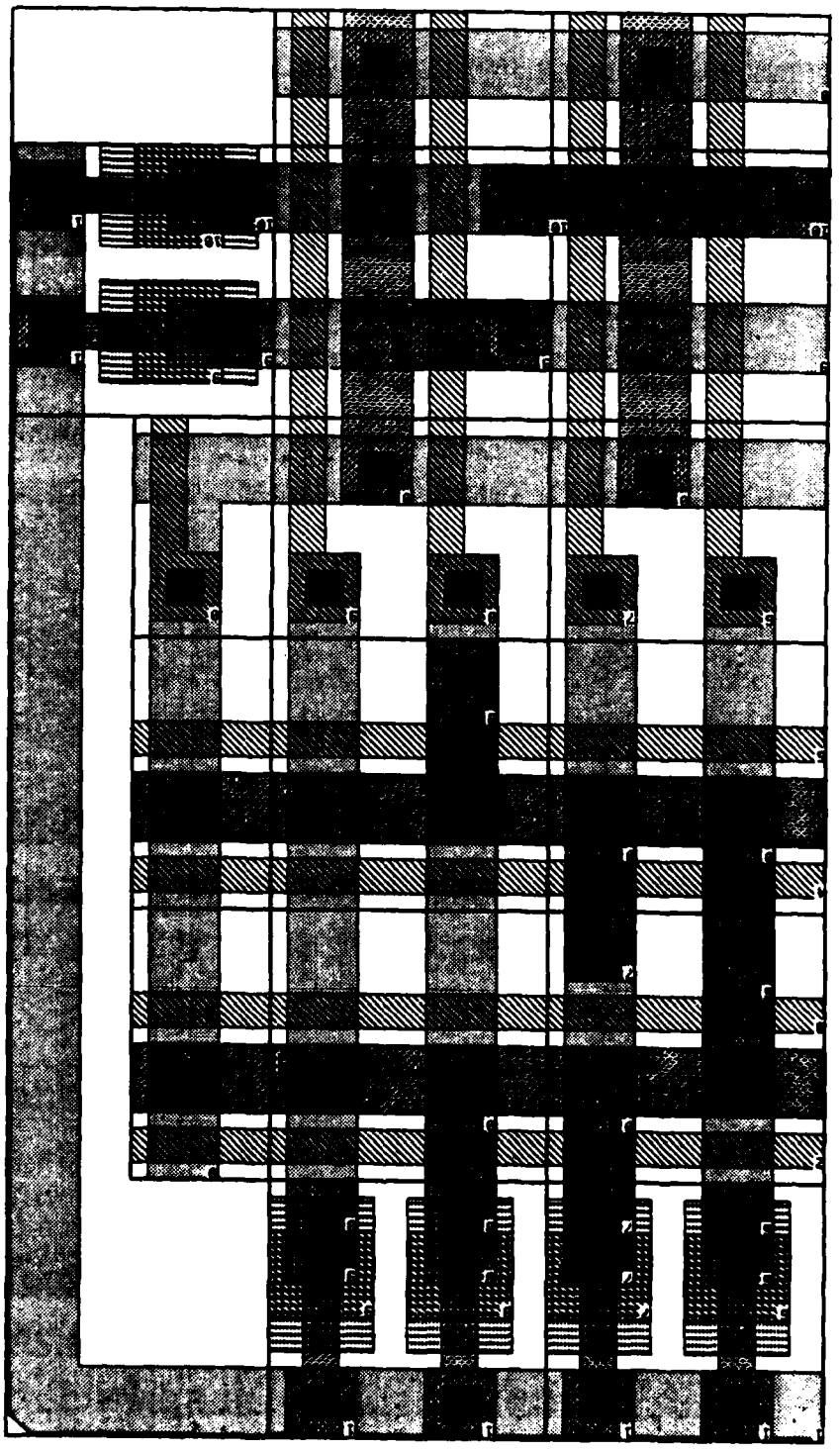


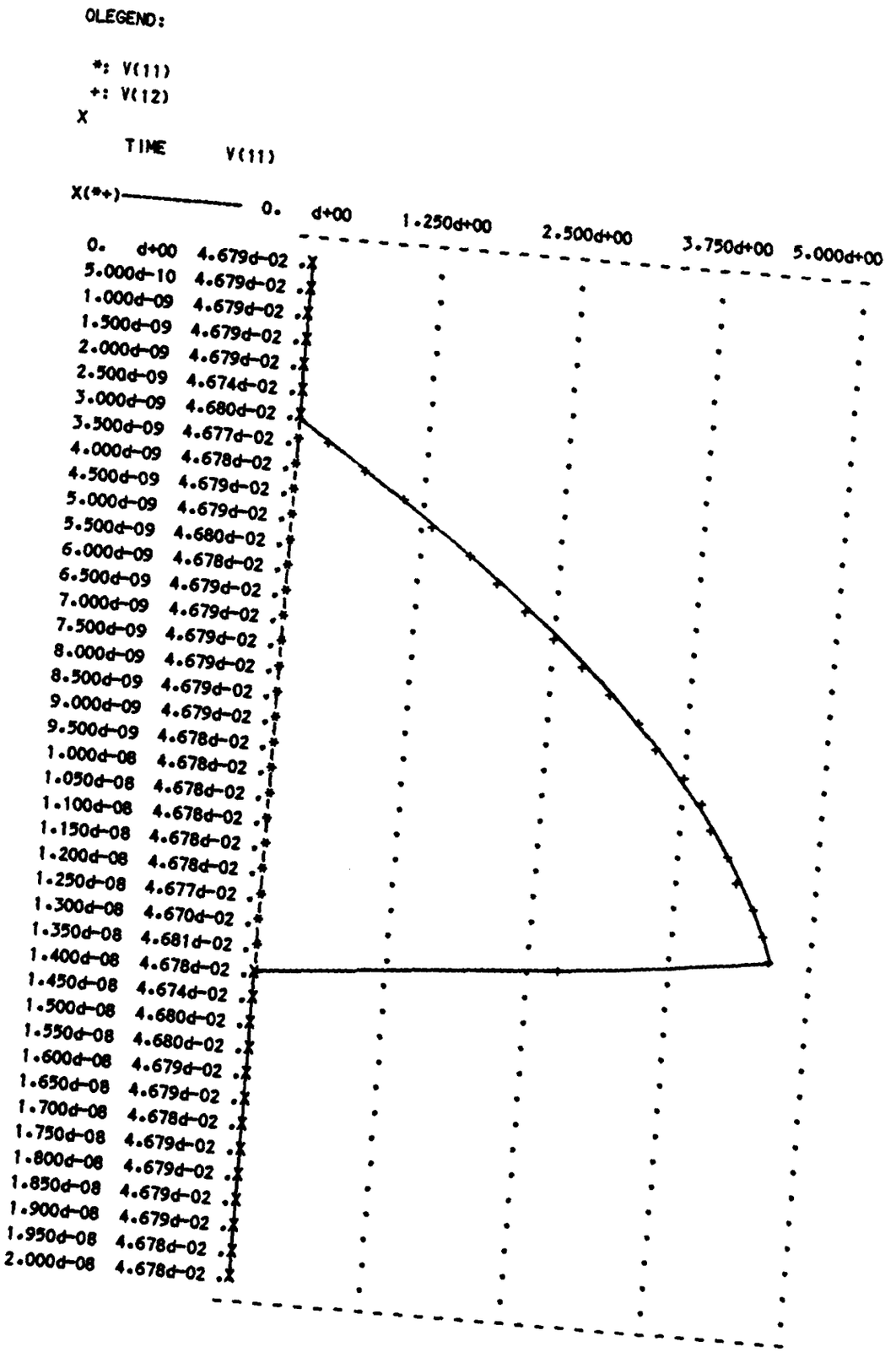
Figure D-4 NMOS PLA Layout With Labeled Nodes

```
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:26:54******

0       NMOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL NE NMOS (VTO=1V KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  .MODEL ND NMOS (VTO=-3.0 KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 8 2 0 0    NE L=2.5UM W=5UM
  MPD2 7 2 0 0    NE L=2.5UM W=5UM
  MPD3 6 3 0 0    NE L=2.5UM W=5UM
  MPD4 6 4 0 0    NE L=2.5UM W=5UM
  MPD5 7 4 0 0    NE L=2.5UM W=5UM
  MPD6 8 5 0 0    NE L=2.5UM W=5UM
  MPD7 10 8 0 0   NE L=2.5UM W=5UM
  MPD8 10 7 0 0   NE L=2.5UM W=5UM
  MPD9 9 6 0 0    NE L=2.5UM W=5UM
  MPD10 11 9 0 0  NE L=2.5UM W=10UM
  MPD11 12 10 0 0 NE L=2.5UM W=10UM
  MPU1 1 6 6 0    ND L=5UM W=2.5UM
  MPU2 1 7 7 0    ND L=5UM W=2.5UM
  MPU3 1 8 8 0    ND L=5UM W=2.5UM
  MPU4 1 9 9 0    ND L=5UM W=2.5UM
  MPU5 1 10 10 0  ND L=5UM W=2.5UM
  MPU6 1 11 11 0  ND L=5UM W=2.5UM
  MPU7 1 12 12 0  ND L=5UM W=2.5UM
  CDBK1 11 0 0.1PF
  CDBK2 12 0 0.1PF
  VIN1 2  0 PULSE (5V 0V 2NS ONS ONS 10NS)
  VIN2 3  0 PULSE (0V 5V 2NS ONS ONS 10NS)
  VIN3 4  0 PULSE (5V 0V 2NS ONS ONS 10NS)
  VIN4 5  0 PULSE (0V 5V 2NS ONS ONS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(11) V(12) (0V,5V)
  .END
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:26:54******

0       NMOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

Simulates first row of truth table.

```
                NE          ND
0TYPE           NMOS        NMOS
0LEVEL          1.000       1.000
0VTO            1.000       -3.000
0KP           2.00d-05    2.00d-05
0GAMMA          0.370       0.370
0PHI            0.540       0.540
0CGSO         3.45d-10    3.45d-10
0CGDO         3.45d-10    3.45d-10
0CJ           7.00d-05    7.00d-05
0CJSW         2.20d-10    2.20d-10
0TOX          1.00d-07    1.00d-07
0NSUB         5.00d+14    5.00d+14
0XJ           1.00d-06    1.00d-06
0LD           1.00d-06    1.00d-06
1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:26:54******

0       NMOS PLA ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    0.        (  4)    5.0000

(  5)    0.        (  6)    0.0934    (  7)    0.0468    (  8)    0.0934

(  9)    5.0000    ( 10)    5.0000    ( 11)    0.0468    ( 12)    0.0468


    VOLTAGE SOURCE CURRENTS

    NAME         CURRENT

    VDD       -3.710d-04

    VIN1       0.   d+00

    VIN2       0.   d+00

    VIN3       0.   d+00

    VIN4       0.   d+00
```

```
     TOTAL POWER DISSIPATION   1.86d-03  WATTS

1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:26:54******

0       NMOS PLA ANALYSIS

0****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*****************************************************************************


0
0**** MOSFETS

0             MPD1       MPD2       MPD3       MPD4       MPD5       MPD6       MPD7
0MODEL        NE         NE         NE         NE         NE         NE         NE
 ID        7.39d-05   3.72d-05   3.61d-14   7.39d-05   3.72d-05   3.61d-14   1.93d-12
 VGS          5.000      5.000      0.         5.000      5.000      0.         0.093
 VDS          0.093      0.047      0.093      0.093      0.047      0.093      5.000
 VBS          0.         0.         0.         0.         0.         0.         0.

0             MPD8       MPD9       MPD10      MPD11      MPU1       MPU2       MPU3
0MODEL        NE         NE         NE         NE         ND         ND         ND
 ID        1.93d-12   1.93d-12   7.44d-05   7.44d-05   7.39d-05   7.44d-05   7.39d-05
 VGS          0.047      0.093      5.000      5.000      0.         0.         0.
 VDS          5.000      5.000      0.047      0.047      4.907      4.953      4.907
 VBS          0.         0.         0.         0.        -0.093     -0.047     -0.093

0             MPU4       MPU5       MPU6       MPU7
0MODEL        ND         ND         ND         ND
 ID        1.57d-11   2.26d-11   7.44d-05   7.44d-05
 VGS          0.         0.         0.         0.
 VDS          0.000      0.000      4.953      4.953
 VBS         -5.000     -5.000     -0.047     -0.047



1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:26:54******

0       NMOS PLA ANALYSIS

0****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*****************************************************************************
```


OLEGEND:
*: V(11)
+: V(12)
X
TIME V(11)
X(*+)
0. d+00
1.250d+00
2.500d+00
3.750d+00
5.000d+00
0. d+00 4.679d-02
5.000d-10 4.679d-02
1.000d-09 4.679d-02
1.500d-09 4.679d-02
2.000d-09 4.679d-02
2.500d-09 4.674d-02
3.000d-09 4.680d-02
3.500d-09 4.677d-02
4.000d-09 4.678d-02
4.500d-09 4.679d-02
5.000d-09 4.679d-02
5.500d-09 4.680d-02
6.000d-09 4.678d-02
6.500d-09 4.679d-02
7.000d-09 4.679d-02
7.500d-09 4.679d-02
8.000d-09 4.679d-02
8.500d-09 4.679d-02
9.000d-09 4.679d-02
9.500d-09 4.678d-02
1.000d-08 4.678d-02
1.050d-08 4.678d-02
1.100d-08 4.678d-02
1.150d-08 4.678d-02
1.200d-08 4.678d-02
1.250d-08 4.677d-02
1.300d-08 4.670d-02
1.350d-08 4.681d-02
1.400d-08 4.678d-02
1.450d-08 4.674d-02
1.500d-08 4.680d-02
1.550d-08 4.680d-02
1.600d-08 4.679d-02
1.650d-08 4.679d-02
1.700d-08 4.678d-02
1.750d-08 4.679d-02
1.800d-08 4.679d-02
1.850d-08 4.679d-02
1.900d-08 4.679d-02
1.950d-08 4.678d-02
2.000d-08 4.678d-02

```
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:38:42*****

0       NMOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL NE NMOS (VTO=1V KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  .MODEL ND NMOS (VTO=-3.0 KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 8 2 0 0    NE L=2.5UM W=5UM
  MPD2 7 2 0 0    NE L=2.5UM W=5UM
  MPD3 6 3 0 0    NE L=2.5UM W=5UM
  MPD4 6 4 0 0    NE L=2.5UM W=5UM
  MPD5 7 4 0 0    NE L=2.5UM W=5UM
  MPD6 8 5 0 0    NE L=2.5UM W=5UM
  MPD7 10 8 0 0   NE L=2.5UM W=5UM
  MPD8 10 7 0 0   NE L=2.5UM W=5UM
  MPD9 9 6 0 0    NE L=2.5UM W=5UM
  MPD10 11 9 0 0  NE L=2.5UM W=10UM
  MPD11 12 10 0 0 NE L=2.5UM W=10UM
  MPU1 1 6 6 0    ND L=5UM W=2.5UM
  MPU2 1 7 7 0    ND L=5UM W=2.5UM
  MPU3 1 8 8 0    ND L=5UM W=2.5UM
  MPU4 1 9 9 0    ND L=5UM W=2.5UM
  MPU5 1 10 10 0  ND L=5UM W=2.5UM
  MPU6 1 11 11 0  ND L=5UM W=2.5UM
  MPU7 1 12 12 0  ND L=5UM W=2.5UM
  CDBK1 11 0 0.1PF
  CDBK2 12 0 0.1PF
  VIN1 2  0 PULSE (5V 0V 2NS 0NS 0NS 10NS)
  VIN2 3  0 PULSE (0V 5V 2NS 0NS 0NS 10NS)
  VIN3 4  0 PULSE (0V 5V 2NS 0NS 0NS 10NS)
  VIN4 5  0 PULSE (5V 0V 2NS 0NS 0NS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(11) V(12) (0V,5V)
  .END
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:38:42*****

0       NMOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

Simulates second row of truth table.

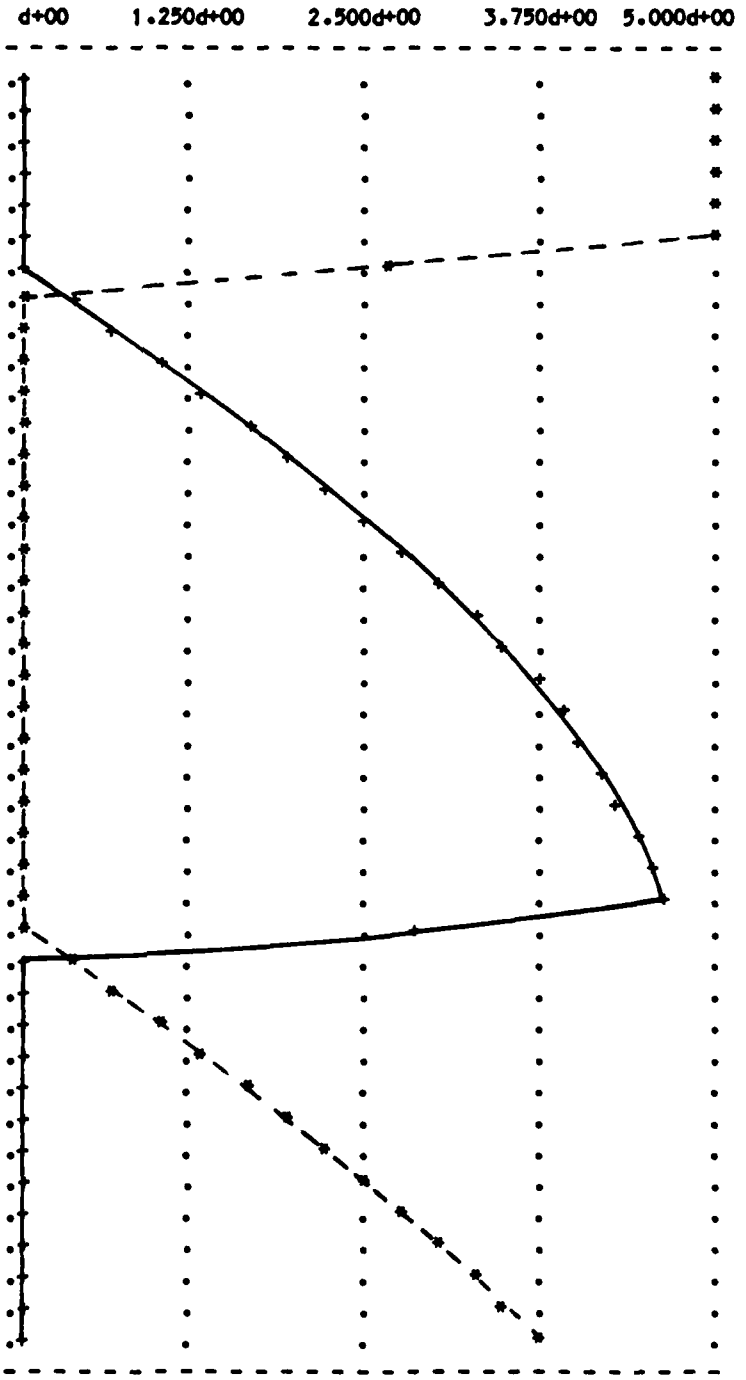
```
                NE          ND
OTYPE           NMOS        NMOS
OLEVEL           1.000       1.000
OVTO             1.000      -3.000
OKP           2.00d-05    2.00d-05
OGAMMA           0.370       0.370
OPHI             0.540       0.540
OCGSO         3.45d-10    3.45d-10
OCGDO         3.45d-10    3.45d-10
OCJ           7.00d-05    7.00d-05
OCJSW         2.20d-10    2.20d-10
OTOX          1.00d-07    1.00d-07
ONSUB         5.00d+14    5.00d+14
OXJ           1.00d-06    1.00d-06
OLD           1.00d-06    1.00d-06
1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:38:42******

0       NMOS PLA ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    5.0000    (  3)    0.        (  4)    0.

(  5)    5.0000    (  6)    5.0000    (  7)    0.0934    (  8)    0.0468

(  9)    0.0934    ( 10)    5.0000    ( 11)    5.0000    ( 12)    0.0468


    VOLTAGE SOURCE CURRENTS

    NAME         CURRENT

    VDD       -2.966d-04

    VIN1       0.   d+00

    VIN2       0.   d+00

    VIN3       0.   d+00

    VIN4       0.   d+00
```

```
     TOTAL POWER DISSIPATION   1.48d-03  WATTS

1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:38:42*****

0       NMOS PLA ANALYSIS

0*****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

0*************************************************************************


0
0***** MOSFETS


0            MPD1       MPD2       MPD3       MPD4       MPD5       MPD6       MPD7
0MODEL     NE         NE         NE         NE         NE         NE         NE
 ID        3.72d-05   7.39d-05   1.93d-12   1.93d-12   3.61d-14   3.72d-05   1.93d-12
 VGS          5.000      5.000      0.         0.         0.         5.000      0.047
 VDS          0.047      0.093      5.000      5.000      0.093      0.047      5.000
 VBS          0.         0.         0.         0.         0.         0.         0.


0            MPD8       MPD9       MPD10      MPD11      MPU1       MPU2       MPU3
0MODEL     NE         NE         NE         NE         ND         ND         ND
 ID        1.93d-12   7.39d-05   1.93d-12   7.44d-05   2.26d-11   7.39d-05   7.44d-05
 VGS          0.093      5.000      0.093      5.000      0.         0.         0.
 VDS          5.000      0.093      5.000      0.047      0.000      4.907      4.953
 VBS          0.         0.         0.         0.        -5.000     -0.093     -0.047


0            MPU4       MPU5       MPU6       MPU7
0MODEL     ND         ND         ND         ND
 ID        7.39d-05   2.26d-11   1.58d-11   7.44d-05
 VGS          0.         0.         0.         0.
 VDS          4.907      0.000      0.000      4.953
 VBS         -0.093     -5.000     -5.000     -0.047


1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:38:42*****

0       NMOS PLA ANALYSIS

0*****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

0*************************************************************************
```

OLEGEND:

*: V(11)
+: V(12)
X

TIME	V(11)
0. d+00	5.000d+00
5.000d-10	5.000d+00
1.000d-09	5.000d+00
1.500d-09	5.000d+00
2.000d-09	5.000d+00
2.500d-09	5.035d+00
3.000d-09	2.693d+00
3.500d-09	9.054d-02
4.000d-09	4.944d-02
4.500d-09	4.710d-02
5.000d-09	4.679d-02
5.500d-09	4.680d-02
6.000d-09	4.681d-02
6.500d-09	4.681d-02
7.000d-09	4.683d-02
7.500d-09	4.683d-02
8.000d-09	4.677d-02
8.500d-09	4.674d-02
9.000d-09	4.676d-02
9.500d-09	4.678d-02
1.000d-08	4.678d-02
1.050d-08	4.678d-02
1.100d-08	4.677d-02
1.150d-08	4.679d-02
1.200d-08	4.679d-02
1.250d-08	4.681d-02
1.300d-08	4.699d-02
1.350d-08	7.528d-02
1.400d-08	4.198d-01
1.450d-08	7.506d-01
1.500d-08	1.070d+00
1.550d-08	1.378d+00
1.600d-08	1.678d+00
1.650d-08	1.970d+00
1.700d-08	2.255d+00
1.750d-08	2.532d+00
1.800d-08	2.800d+00
1.850d-08	3.056d+00
1.900d-08	3.296d+00
1.950d-08	3.517d+00
2.000d-08	3.719d+00



```
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:39:28******

0       NMOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************

  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL NE NMOS (VTO=1V KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  .MODEL ND NMOS (VTO=-3.0 KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 8 2 0 0    NE L=2.5UM W=5UM
  MPD2 7 2 0 0    NE L=2.5UM W=5UM
  MPD3 6 3 0 0    NE L=2.5UM W=5UM
  MPD4 6 4 0 0    NE L=2.5UM W=5UM
  MPD5 7 4 0 0    NE L=2.5UM W=5UM
  MPD6 8 5 0 0    NE L=2.5UM W=5UM
  MPD7 10 8 0 0   NE L=2.5UM W=5UM
  MPD8 10 7 0 0   NE L=2.5UM W=5UM
  MPD9 9 6 0 0    NE L=2.5UM W=5UM
  MPD10 11 9 0 0  NE L=2.5UM W=10UM
  MPD11 12 10 0 0 NE L=2.5UM W=10UM
  MPU1 1 6 6 0    ND L=5UM W=2.5UM
  MPU2 1 7 7 0    ND L=5UM W=2.5UM
  MPU3 1 8 8 0    ND L=5UM W=2.5UM
  MPU4 1 9 9 0    ND L=5UM W=2.5UM
  MPU5 1 10 10 0  ND L=5UM W=2.5UM
  MPU6 1 11 11 0  ND L=5UM W=2.5UM
  MPU7 1 12 12 0  ND L=5UM W=2.5UM
  CDBK1 11 0 0.1PF
  CDBK2 12 0 0.1PF
  VIN1 2  0 PULSE (0V 5V 2NS ONS ONS 10NS)   Simulates third row
  VIN2 3  0 PULSE (5V 0V 2NS ONS ONS 10NS)   of truth table.
  VIN3 4  0 PULSE (5V 0V 2NS ONS ONS 10NS)
  VIN4 5  0 PULSE (0V 5V 2NS ONS ONS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(11) V(12) (0V,5V)
  .END
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:39:28******

0       NMOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
                NE          ND
0TYPE           NMOS        NMOS
0LEVEL           1.000       1.000
0VTO             1.000      -3.000
0KP           2.00d-05    2.00d-05
0GAMMA           0.370       0.370
0PHI             0.540       0.540
0CGSO         3.45d-10    3.45d-10
0CGDO         3.45d-10    3.45d-10
0CJ           7.00d-05    7.00d-05
0CJSW         2.20d-10    2.20d-10
0TOX          1.00d-07    1.00d-07
0NSUB         5.00d+14    5.00d+14
0XJ           1.00d-06    1.00d-06
0LD           1.00d-06    1.00d-06
1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:39:28******

0       NMOS PLA ANALYSIS

0*****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    0.        (  3)    5.0000    (  4)    5.0000

(  5)    0.        (  6)    0.0468    (  7)    0.0934    (  8)    5.0000

(  9)    5.0000    ( 10)    0.0934    ( 11)    0.0468    ( 12)    5.0000


     VOLTAGE SOURCE CURRENTS

     NAME         CURRENT

     VDD       -2.966d-04

     VIN1       0.   d+00

     VIN2       0.   d+00

     VIN3       0.   d+00

     VIN4       0.   d+00
```

TOTAL POWER DISSIPATION 1.48d-03 WATTS

1*******09/30/83 ******** SPICE 2G.1 (15OCT80) ********21:39:28*****

0 NMOS PLA ANALYSIS

0**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

0**********

0

0**** MOSFETS

0	MPD1	MPD2	MPD3	MPD4	MPD5	MPD6	MPD7
0MODEL	NE	NE	NE	NE	NE	NE	NE
ID	1.93d-12	3.61d-14	3.72d-05	3.72d-05	7.39d-05	1.93d-12	7.39d-05
VGS	0.	0.	5.000	5.000	5.000	0.	5.000
VDS	5.000	0.093	0.047	0.047	0.093	5.000	0.093
VBS	0.	0.	0.	0.	0.	0.	0.

0	MPD8	MPD9	MPD10	MPD11	MPU1	MPU2	MPU3
0MODEL	NE	NE	NE	NE	ND	ND	ND
ID	3.61d-14	1.93d-12	7.44d-05	1.93d-12	7.44d-05	7.39d-05	2.26d-11
VGS	0.093	0.047	5.000	0.093	0.	0.	0.
VDS	0.093	5.000	0.047	5.000	4.953	4.907	0.000
VBS	0.	0.	0.	0.	-0.047	-0.093	-5.000

0	MPU4	MPU5	MPU6	MPU7
0MODEL	ND	ND	ND	ND
ID	1.57d-11	7.39d-05	7.44d-05	1.58d-11
VGS	0.	0.	0.	0.
VDS	0.000	4.907	4.953	0.000
VBS	-5.000	-0.093	-0.047	-5.000

1*******09/30/83 ******** SPICE 2G.1 (15OCT80) ********21:39:28*****

0 NMOS PLA ANALYSIS

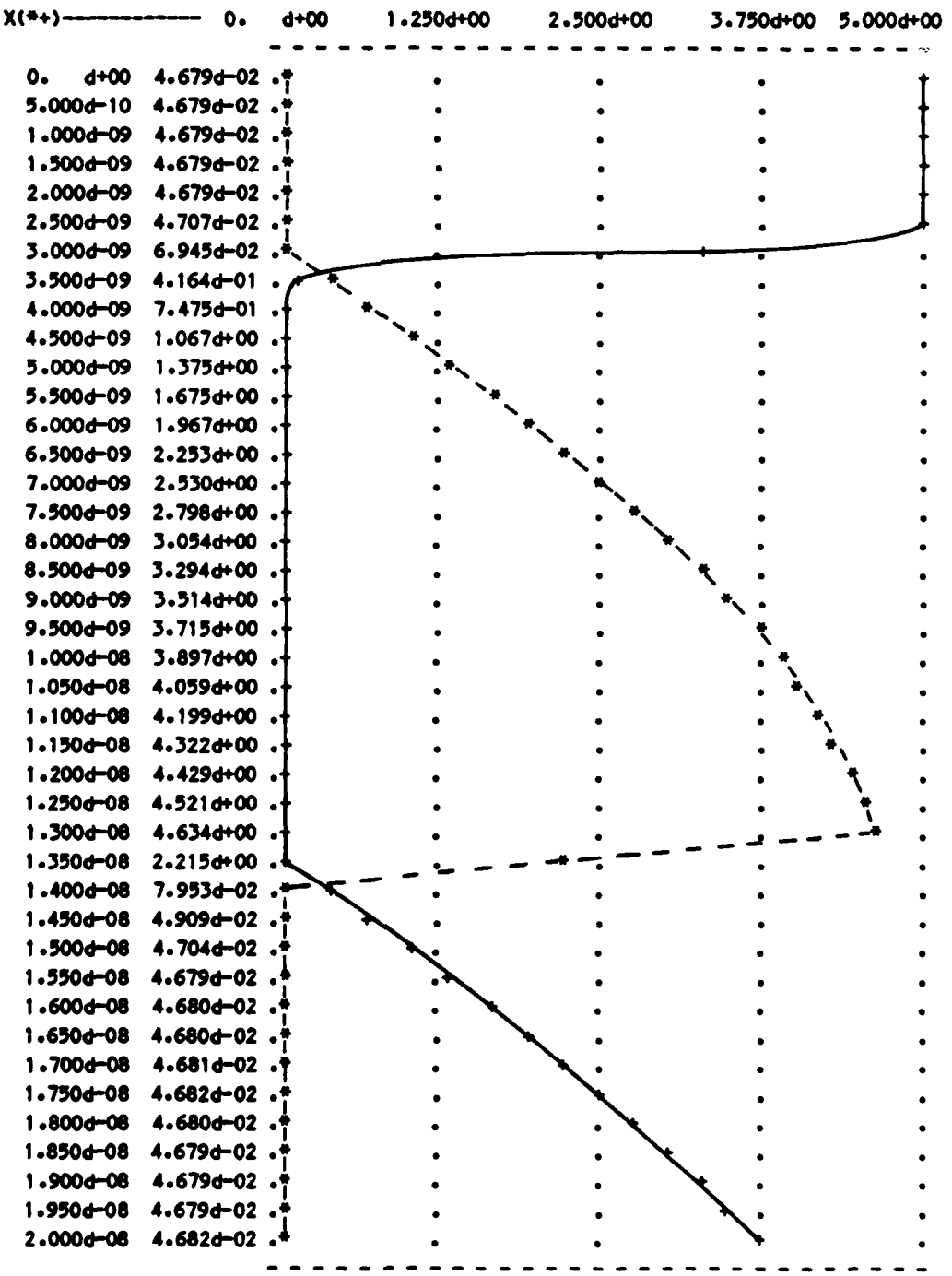
0**** TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

0**********

OLEGEND:

*: V(11)
+: V(12)
X

TIME	V(11)
0. d+00	4.679d-02
5.000d-10	4.679d-02
1.000d-09	4.679d-02
1.500d-09	4.679d-02
2.000d-09	4.679d-02
2.500d-09	4.707d-02
3.000d-09	6.945d-02
3.500d-09	4.164d-01
4.000d-09	7.475d-01
4.500d-09	1.067d+00
5.000d-09	1.375d+00
5.500d-09	1.675d+00
6.000d-09	1.967d+00
6.500d-09	2.253d+00
7.000d-09	2.530d+00
7.500d-09	2.798d+00
8.000d-09	3.054d+00
8.500d-09	3.294d+00
9.000d-09	3.514d+00
9.500d-09	3.715d+00
1.000d-08	3.897d+00
1.050d-08	4.059d+00
1.100d-08	4.199d+00
1.150d-08	4.322d+00
1.200d-08	4.429d+00
1.250d-08	4.521d+00
1.300d-08	4.634d+00
1.350d-08	2.215d+00
1.400d-08	7.953d-02
1.450d-08	4.909d-02
1.500d-08	4.704d-02
1.550d-08	4.679d-02
1.600d-08	4.680d-02
1.650d-08	4.680d-02
1.700d-08	4.681d-02
1.750d-08	4.682d-02
1.800d-08	4.680d-02
1.850d-08	4.679d-02
1.900d-08	4.679d-02
1.950d-08	4.679d-02
2.000d-08	4.682d-02



```
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:40:26******

0       NMOS PLA ANALYSIS

0****     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

0******************************************************************************


  .WIDTH OUT=80
  .OPTIONS ITL1=500 ITL5=0
  .MODEL NE NMOS (VTO=1V KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  .MODEL ND NMOS (VTO=-3.0 KP=20E-6 GAMMA=0.37 NSUB=5E14 TOX=0.1UM
  +XJ=1.0UM LD=1.0UM CJ=70UF CJSW=220PF CGSO=345PF CGDO=345PF)
  +LEVEL=1
  VDD 1 0 DC 5V
  MPD1 8 2 0 0    NE L=2.5UM W=5UM
  MPD2 7 2 0 0    NE L=2.5UM W=5UM
  MPD3 6 3 0 0    NE L=2.5UM W=5UM
  MPD4 6 4 0 0    NE L=2.5UM W=5UM
  MPD5 7 4 0 0    NE L=2.5UM W=5UM
  MPD6 8 5 0 0    NE L=2.5UM W=5UM
  MPD7 10 8 0 0   NE L=2.5UM W=5UM
  MPD8 10 7 0 0   NE L=2.5UM W=5UM
  MPD9 9 6 0 0    NE L=2.5UM W=5UM
  MPD10 11 9 0 0  NE L=2.5UM W=10UM
  MPD11 12 10 0 0 NE L=2.5UM W=10UM
  MPU1 1 6 6 0    ND L=5UM W=2.5UM
  MPU2 1 7 7 0    ND L=5UM W=2.5UM
  MPU3 1 8 8 0    ND L=5UM W=2.5UM
  MPU4 1 9 9 0    ND L=5UM W=2.5UM
  MPU5 1 10 10 0  ND L=5UM W=2.5UM
  MPU6 1 11 11 0  ND L=5UM W=2.5UM
  MPU7 1 12 12 0  ND L=5UM W=2.5UM
  CDBK1 11 0 0.1PF
  CDBK2 12 0 0.1PF
  VIN1 2  0 PULSE (0V 5V 2NS 0NS 0NS 10NS)   Simulates last row
  VIN2 3  0 PULSE (5V 0V 2NS 0NS 0NS 10NS)   of truth table.
  VIN3 4  0 PULSE (0V 5V 2NS 0NS 0NS 10NS)
  VIN4 5  0 PULSE (5V 0V 2NS 0NS 0NS 10NS)
  .TRAN 0.5NS 20NS
  .PLOT TRAN V(11) V(12) (0V,5V)
  .END
1*******09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:40:26******

0       NMOS PLA ANALYSIS

0****     MOSFET MODEL PARAMETERS          TEMPERATURE =   27.000 DEG C

0******************************************************************************
```

```
                NE          ND
0TYPE           NMOS        NMOS
0LEVEL          1.000       1.000
0VTO            1.000       -3.000
0KP           2.00d-05    2.00d-05
0GAMMA          0.370       0.370
0PHI            0.540       0.540
0CGSO         3.45d-10    3.45d-10
0CGDO         3.45d-10    3.45d-10
0CJ           7.00d-05    7.00d-05
0CJSW         2.20d-10    2.20d-10
0TOX          1.00d-07    1.00d-07
0NSUB         5.00d+14    5.00d+14
0XJ           1.00d-06    1.00d-06
0LD           1.00d-06    1.00d-06
1********09/30/83 ********  SPICE 2G.1 (15OCT80)  ********21:40:26******

0       NMOS PLA ANALYSIS

0****     INITIAL TRANSIENT SOLUTION       TEMPERATURE =   27.000 DEG C

0*****************************************************************************

  NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(  1)    5.0000    (  2)    0.        (  3)    5.0000    (  4)    0.

(  5)    5.0000    (  6)    0.0934    (  7)    5.0000    (  8)    0.0934

(  9)    5.0000    ( 10)    0.0934    ( 11)    0.0468    ( 12)    5.0000


    VOLTAGE SOURCE CURRENTS

    NAME         CURRENT

    VDD       -2.961d-04

    VIN1       0.   d+00

    VIN2       0.   d+00

    VIN3       0.   d+00

    VIN4       0.   d+00
```

TOTAL POWER DISSIPATION 1.48d-03 WATTS

1********09/30/83 ******** SPICE 2G.1 (15OCT80) ********21:40:26*****

0 NMOS PLA ANALYSIS

0***** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

0**********

0

0***** MOSFETS

0	MPD1	MPD2	MPD3	MPD4	MPD5	MPD6	MPD7
OMODEL	NE	NE	NE	NE	NE	NE	NE
ID	3.61d-14	1.93d-12	7.39d-05	3.61d-14	1.93d-12	7.39d-05	3.61d-14
VGS	0.	0.	5.000	0.	0.	5.000	0.093
VDS	0.093	5.000	0.093	0.093	5.000	0.093	0.093
VBS	0.	0.	0.	0.	0.	0.	0.

0	MPD8	MPD9	MPD10	MPD11	MPU1	MPU2	MPU3
OMODEL	NE	NE	NE	NE	ND	ND	ND
ID	7.39d-05	1.93d-12	7.44d-05	1.93d-12	7.39d-05	2.26d-11	7.39d-05
VGS	5.000	0.093	5.000	0.093	0.	0.	0.
VDS	0.093	5.000	0.047	5.000	4.907	0.000	4.907
VBS	0.	0.	0.	0.	-0.093	-5.000	-0.093

0	MPU4	MPU5	MPU6	MPU7
OMODEL	ND	ND	ND	ND
ID	1.57d-11	7.39d-05	7.44d-05	1.58d-11
VGS	0.	0.	0.	0.
VDS	0.000	4.907	4.953	0.000
VBS	-5.000	-0.093	-0.047	-5.000

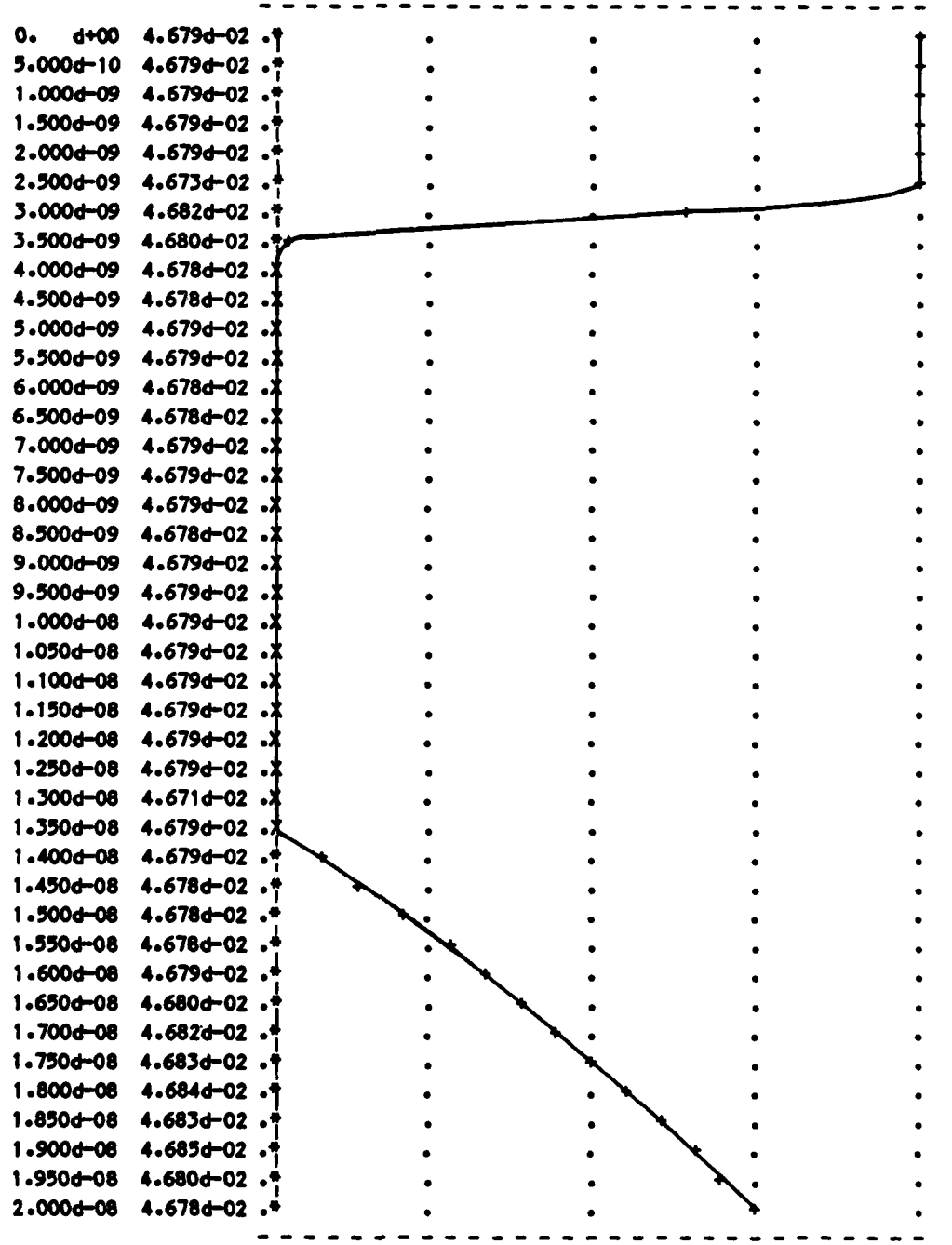
1********09/30/83 ******** SPICE 2G.1 (15OCT80) ********21:40:26*****

0 NMOS PLA ANALYSIS

0***** TRANSIENT ANALYSIS TEMPERATURE = 27.000 DEG C

0**********

```
OLEGEND:

 *: V(11)
 +: V(12)
X
     TIME        V(11)

X(*+)————————— 0.   d+00      1.250d+00      2.500d+00      3.750d+00  5.000d+00
```



```
  0.   d+00   4.679d-02 .*
 5.000d-10   4.679d-02 .*
 1.000d-09   4.679d-02 .*
 1.500d-09   4.679d-02 .*
 2.000d-09   4.679d-02 .*
 2.500d-09   4.673d-02 .*
 3.000d-09   4.682d-02 .*
 3.500d-09   4.680d-02 .*
 4.000d-09   4.678d-02 .X
 4.500d-09   4.678d-02 .X
 5.000d-09   4.679d-02 .X
 5.500d-09   4.679d-02 .X
 6.000d-09   4.678d-02 .X
 6.500d-09   4.678d-02 .X
 7.000d-09   4.679d-02 .X
 7.500d-09   4.679d-02 .X
 8.000d-09   4.679d-02 .X
 8.500d-09   4.678d-02 .X
 9.000d-09   4.679d-02 .X
 9.500d-09   4.679d-02 .X
 1.000d-08   4.679d-02 .X
 1.050d-08   4.679d-02 .X
 1.100d-08   4.679d-02 .X
 1.150d-08   4.679d-02 .X
 1.200d-08   4.679d-02 .X
 1.250d-08   4.679d-02 .X
 1.300d-08   4.671d-02 .X
 1.350d-08   4.679d-02 .X
 1.400d-08   4.679d-02 .*
 1.450d-08   4.678d-02 .*
 1.500d-08   4.678d-02 .*
 1.550d-08   4.678d-02 .*
 1.600d-08   4.679d-02 .*
 1.650d-08   4.680d-02 .*
 1.700d-08   4.682d-02 .*
 1.750d-08   4.683d-02 .*
 1.800d-08   4.684d-02 .*
 1.850d-08   4.683d-02 .*
 1.900d-08   4.685d-02 .*
 1.950d-08   4.680d-02 .*
 2.000d-08   4.678d-02 .*
```

Appendix E. Software Implementation/Testing

Implementation and testing of the CMOS/SOS PLA generator "cplagen" are discussed. Also addressed are the procedures required to use cplagen to produce a CIF representation of a CMOS/SOS PLA. All source code is provided and is documented to simplify future modifications.

Implementation

Most modules were coded as represented by their structure charts in Chapter IV and Chapter V. Some modules however, were not broken down into separate functions because they were more easily integrated into larger modules. In these instances, only the location of the code that performs the function of the smaller module is identified. Because no specific algorithm is available for this type of computer-aided design software, the structure charts were made more detailed than was probably necessary. The goal was to provide the beginning CAD designer with a detailed graphical representation of the procedures necessary to generate the CMOS/SOS PLA.

Testing

Various size PLAs, with and without options, have been plotted to test the specifications presented in Chapter III. In all cases, the plots were manually inspected to verify accuracy of the layout. Additionally, several CIF representations were tested for design rule violations by using the NMOS design rule checker. Interestingly, no

errors were detected, including implant surround errors. NMOS implant requirements are not the same as those required by the CMOS/SOS process, which usually results in numerous errors. Most standard cells, for example, have numerous errors. Yet, because of the layout of the PLA, none were detected for any of the test cases.

Sizes of the test PLAs were calculated manually to verify accuracy of the information sent to the user's terminal. Calculations verified program-generated data for all test cases. Limited bounds testing was employed to test for error detection. As an example, a 1x1x0 PLA (the smallest possible) was generated and plotted correctly. But a 0x0x0 input produced an error message, and the program aborted. Upper bounds were not tested due the time required to create the input file for an extremely large PLA (100x200x100 for example). The applicability and physical operational integrity of such a large PLA is questionable anyway.

Only one error situation was detected which involves specification of the CMOS/SOS geometry in the cplagen input file. If 4.0 micron geometry is specified rather than 2.5 as for the NMOS process, CIF round-off errors will occur when the file is processed by CLL. CLL documentation states that number resolution is half of a lambda. More simply, 0.5 is legal but 0.25 is not [Ref 3]. Why the specification of 2.5 for NMOS PLAs is acceptable, but the specification of 4.0 for CMOS/SOS PLAs causes round-off errors, is uncertain.

A possible alternative is to use 2.5 in the PLA input file, then change the specification in the file "final.cif" back to 4.0. This procedure is not guaranteed, nor can the results of the fabrication be predicted. Some debugging was attempted to try to correct the problem but with no positive results. As an example, all coordinates that required fractional parts of 0.5 were changed to whole numbers, but round-off errors still occurred. This author suspects that CLL is coded to accept only 2.5 lambda geometries without modifications.

To verify this assumption, several test PLAs were processed by CLL using a 2.5 lambda. All references to 2.5 lambda were then removed from the resulting CIF formatted file. Additionally, all references to lambda in the PLA cell library were changed to reflect a 4.0 lambda (1.25 was globally replaced with 2.00 in "total.cif". Note: CLL processed CIF files reference lambda as lambda divided by two "lambda/2"). These CIF formatted files were plotted using Berkeley's CIFPLOT with varying scaling factors. In all cases, CIFPLOT produced the correct PLA plot with no CIF warnings or errors. Even greatly enlarged CIF plots showed no signs of round-off errors. Thus, since CIFPLOT is based upon the same CIF interpretation rules as those used for fabrication, CMOS/SOS PLAs should fabricate correctly.

The only constraint imposed upon the user will be to postpone specification of 4.0 lambda for any designs until the "final.cif" file is created.

File Name:

cplagen

Calling Syntax:

cplagen [-options] input output

Description:

Cplagen is an executable program that converts an input file specification for a PLA into a CIF representation of that PLA. The CIF representation is a file formatted in standard CIF 2.0 format. The file contains calls to CMOS/SOS PLA cells (pieces) that are contained in the file "total.cif". Included in "total.cif" are all the PLA cells necessary to generate any size PLA with or without options. Only the NAND/NAND form of the PLA is generated without folding or interleaving. Four sample PLAs, all 3x4x4, are plotted and labled (see Figures E-1 through E-4) to show the basic PLA with no clocking options, and also with various stages of clocking options added.

Options

-i	clock only PLA inputs
-o	clock only PLA outputs
-b	clock both PLA inputs and PLA outputs

The input file to cplagen specifies the size of the PLA, the PLA symbol number, and the geometry as well as the PLA truth table. The format is as follows:

```
#inputs, #product terms, #outputs, symbol#, lambda
xxxxxxxxxxxx yyyyyyyyyyyyyyy
xxxxxxxxxxxx yyyyyyyyyyyyyyy
xxxxxxxxxxxx yyyyyyyyyyyyyyy
xxxxxxxxxxxx yyyyyyyyyyyyyyy
```

where: #inputs is the number of inputs to the PLA.
#product terms is the number of PLA product terms
#outputs is the number of outputs in the PLA.
symbol# is the CIF ID assigned to the PLA.
#lambda is the current geometry for CMOS/SOS in microns (note: because of bug, only 2.5 will work)
x represents inputs
y represents outputs

The PLA cells use CIF symbol numbers 959 through 974. Do not identify your PLA with one of these numbers. Any other number between 900 and 999 is acceptable.

The PLA truth table is encoded as follows:

INPUTS---three possible conditions:

1. If term is a "don't care term", use a dash "-"
2. If term is true if input is true, use a one "1"
3. If term is true if input is false, use a zero "0"

OUTPUTS---two possible conditions

1. If output depends on this term, use a dash "-"
2. If output is not affected by this term, use a zero "0"

Example for Figure E-1 (page E-20): Use a PLA to implement the

following functions (simplification is not used):

z1 = a
z2 = a + a'b'c
z3 = b'c'
z4 = a'b'c + a'bc'

The PLA will have 3 inputs (a, b, c), four product terms R1-R4 (because there are four different products of sums a, b'c, a'bc', and a'b'c), and four outputs (z1, z2, z3, z4). Choose PLA symbol number = 920 and lambda = 2.5. The input file is arranged as follows:

```
3,4,4,920,2.5
1-- --00
-00 00-0
001 0-0-
010 000-
```

Note: When using CLL to obtain a plot, you must include the file "total.cif" on the CLL command line.

Cplagen will automatically generate the output file and send two lines to the user's terminal. The first line verifies the number of inputs, outputs, and product terms. For the above example the screen would show:

```
3 input 4 output 4 term PLA
```

The second line contains the calculated size of the PLA. For the above example, the screen would show:

```
external pla (cif 920 bounds 0,0 162,97)
```

Error checking routines look for disallowed characters and premature end of file or premature end of line. Note: the number of inputs, product terms, and outputs must match the PLA truth table to prevent errors.

```
/*****************************************************************
*                                                               *
*       DATE:  20 Sept 83                                       *
*       VERSION:  1.0                                           *
*       TITLE:  CMOS/SOS Pla Generator                          *
*       FILENAME:  cplagen.c                                    *
*       OWNER:  W. SOMMARS                                      *
*       SOFTWARE SYSTEM:  VAX/11-780                            *
*       OPERATING SYSTEM:  BERKELEY VAX/UNIX 4.1bsd             *
*       USE:  This file was written to be compiled with the VAX/11-780 *
*             'C' compiler.  Input and output are as follows:   *
*                                                               *
*       cplagen -[] input output                                *
*           input  filename (pla specifications) (default:stdin)*
*           output filename (generated CIF for Pla) (default:stdout) *
*           -i  clock only Pla inputs                           *
*           -o  clock only Pla outputs                          *
*           -b  clock both Pla inputs and Pla outputs           *
*                                                               *
*       CONTENTS:  main, errcheck, cifwrite, proginp, progout, progopt *
*       FUNCTION:  main - opens input and output files, reads command *
*                         line, and generates Pla AND and OR planes. *
*                  errcheck - checks for extraneous characters in *
*                             input file                        *
*                  cifwrite - writes CIF statments to output file *
*                  proginp - generates CIF coordinates for input terms *
*                  progout - generates CIF coordinates for output terms *
*                  progopt - generates CIF coordinates for clock options*
*                                                               *
*****************************************************************/


/*****************************************************************
*                                                               *
*       NAME:  main (Generate CMOS/SOS PLA)                     *
*       MODULE NUMBER:  1.0  (includes modules 1.2 initiate CIF File, *
*                       1.3 Assemble PLA Pieces, 1.3.1 Assemble PLA *
*                       Planes, and 1.4 Terminate CIF File)     *
*       FUNCTION:  calls subordinate modules used to generate file *
*                  formatted in CIF.  does preliminary error checking. *
*       INPUTS:  stdin or input file                            *
*       OUTPUTS:  none                                          *
*       CALLING MODULES:  none                                  *
*       MODULES CALLED:  1.1 errcheck (Error Check), 1.3.2 proginp/ *
*                        progout (Program I/O Terms), 1.3.3 progopt *
*                        (Program Clocking Options), and 1.3.1.1.1 *
*                        cifwrite (Write to CIF File)           *
*                                                               *
*****************************************************************/
```

```
#include stdio.h


/* AFIT CMOS/SOS library PLA cell symbols */
#define NMOS        962      /* Pla NMOS Transistor */
#define CCONNE1     963      /* Pla Connect1 */
#define PMOS        964      /* Pla PMOS transistor */
#define CGNDCON     965      /* Pla Ground Connect */
#define NSPACE      966      /* Pla NMOS Space */
#define CCELL       967      /* Pla Cell Left */
#define CCELLR      968      /* Pla Cell Right */
#define CCELLSP     969      /* Pla Cell Space */
#define CCONNE2     970      /* Pla Connect2 */
#define PlaOut      971      /* Pla Output */
#define CCONNE3     972      /* Pla Connect3 */
#define HOLESP1     973      /* Pla Hole Space1 */
#define HOLESP2     974      /* Pla Hole Space2 */
#define PlaClkIn    959      /* Pla Clock In */
#define PlaClkOut   960      /* Pla Clock Out */

/* Cell pitch in units of lambda */
#define LNMOS        14      /* NMOS Cell length */
#define LCCELL       20      /* Pla Cell width*/
#define WCCELL       21      /* Pla Cell width*/
#define LCCELLR      21      /* Pla Cell right length */
#define WCCELLR      14      /* Pla Cell right width */
#define WCCELLSP      7      /* Pla Cell space width */
#define LCGNDCON      3      /* Pla Ground Connect length */
#define LHOLESP2     10      /* Pla Hole Space2 length */
#define LPlaClkIn    20      /* Pla Clock In width */
#define WPlaClkIn    48      /* Pla Clock In Length */
#define LPlaClkOut   21      /* Pla Clock Out length */
#define WPlaClkOut   27      /* Pla Clock Out width */


main(argc,argv)          /* read pla specifications from input file */
  int argc;
  char *argv[];
  {
        FILE *fopen(), *fpi, *fpo;

        int inputs, terms, outputs, symbnm;
        float rlamb;                              /* lambda in microns */
        char *pterm[1],*ptag[1];
        int row, col, lambda;
        int i, j, ixsize, iysize;
        int x, y, x1, y1, x2, y2, x3, y3;
        int clfwrite();
        char line[200];
        char interm[100], outerm[100];
        int icheck;
        char *pcheck;
        int clkin = 0;
```

```
int clkout = 0;
int clkboth = 0;
char opt;


fpi = stdin;
fpo = stdout;

for (i=j=1; i<argc; i++)        /* determine options */
 {

        if (argv[i][0] == '-')
        {
              opt = argv[i][1];
              switch(opt)
                {
              case 'i':
                      clkin = 1;
                      break;
              case 'o':
                      ++clkout;
                      break;
              case 'b':
                      ++clkboth;
                      break;
                 }
          }

        else switch(j++)        /* argument error checking */
        {
              case 1:
                      if ((fpi=fopen(argv[i],"r")) == NULL)
                        {     fprintf(stderr,"can't open %s\n",
                                      argv[i]);
                              exit(1);
                         }
                      break;
              case 2:
                      if ((fpo=fopen(argv[i],"w")) == NULL)
                        {     fprintf(stderr,"can't open %s\n",
                                      argv[i]);
                              exit(1);
                         }
                      break;
              default:
                  fprintf(stderr,"bad number of file arguments\n");
                  break;
        }

 }

if (fgets(line, 200, fpi) == NULL)
 {
```

```
        fprintf(stderr, "No input or file error n");
        exit(1);
    }

if (sscanf(line,"%d,%d,%d,%d,%f", &inputs, &terms, &outputs,
        &symbnm, &rlamb) != 5)
    {
        fprintf(stderr, "Control line with #_inputs, etc. is bad\n");
        exit(1);
    }

/*****************************************************************
*                                                                *
*    The following implements module 1.2 (Initiate CIF File)    *
*                                                                *
*****************************************************************/

lambda = 100.0*rlamb+0.5;       /* convert lambda to cif units
                                        (0.01 micron) */

/* Write external reference records for CIF loader */

fprintf(fpo,"(ext %d);\n(ext %d);\n(ext %d);\n(ext %d);\n",
    NMOS,CCONNE1,PMOS,CGNDCON);
fprintf(fpo,"(ext %d);\n(ext %d);\n(ext %d);\n(ext %d);\n",
    NSPACE,CCELL,CCELLR,CCELLSP);
fprintf(fpo,"(ext %d);\n(ext %d);\n(ext %d);\n(ext %d);\n",
    CCONNE2,PlaOut,CCONNE3,HOLESP1);
fprintf(fpo,"(ext %d);\n(ext %d);\n(ext %d);\n",
    HOLESP2,PlaClkIn,PlaClkOut);

/* open CIF definition of Pla symbol */
fprintf(fpo,"DS %d %d, 1;\n", symbnm, lambda);

fprintf(stderr,"(%d input %d output %d term PLA);\n", inputs, outputs,
        terms);

/*****************************************************************
*                                                                *
*    The folowing implements module 1.3.1 (Assemble PLA Planes)  *
*    and its subordinate modules 1.3.1.1 (Assemble AND Plane     *
*    Pieces), 1.3.1.2 (Assemble Connecting Pieces), 1.3.1.3      *
*    (Assemble OR Plane Pieces), and 1.3.1.4 (Generate VDD and   *
*    ground busses).                                             *
*                                                                *
*****************************************************************/

for (row = 0; row < terms; row++)       /* generate pla by rows */
  {

     if(fgets(line,200,fpl) == NULL)
      {
          fprintf(stderr,"Premature EOF or file error\n");
          exit(1);
      }
```

```
pterm[1] = &interm[1];
ptag[1] = &outerm[1];

if(sscanf(line,"%s %s",pterm[1],ptag[1]) != 2)
  {
      fprintf(stderr,"Bad input line: %\n",line);
      exit(1);
  }


for (col = 0; col < inputs; col++)    /* program AND plane */
 {

    pcheck = (pterm[1] + col);          /* assign pcheck to */
                                        /* input term */
    errcheck(line, pcheck, '1');        /* check input terms */
                                        /* for errors */
    proginp(fpo,pcheck,row,col,terms); /* prog input terms */


    x = 7 + col*LCCELL;                 /* program CCELL */
    y = 4 + (terms-1)*WCCELL - row*WCCELL;
    clfwrite(fpo,CCELL,x,y,0,0,0);

    if (row == 0 && col ==0)      /* left GND buss wire */
       {
          fprintf(fpo,"L NM; n");
          x1 = x2 = 2;
          y1 = 6.0;
          y2 = terms*WCCELL;
          fprintf(fpo,"W 4 %d,%d %d,%d;\n",x1,y1,x2,y2);
       }

    if((row+1) == terms)    /* program input clock options */
       {
          progopt(fpo,inputs,col,clkin,clkout,clkboth,'1');
       }
 }


x = 4;                    /* PlaGndConnect */
y = terms*WCCELL - row*WCCELL - 3;
clfwrite(fpo,CGNDCON,x,y,0,0,0);

x = 7 + inputs*LCCELL;  /* PlaConnectPieces */
y1 = 11 + (terms-1)*WCCELL - row*WCCELL;
y2 = 4 + (terms-1)*WCCELL - row*WCCELL;
clfwrite(fpo,CCONNE1,x,y1,0,0,0);
clfwrite(fpo,CCONNE2,x,y2,0,0,0);

if (outputs)                          /* program OR plane */
```

```
{
    for (col = 0; col < outputs; col++)
     {

       pcheck = (ptag[1] + col);   /* assign pcheck to */
                                   /* output terms */

       errcheck(line, pcheck, 'o'); /* check output terms */
                                   /* for errors */

       progout(fpo,pcheck,row,col,terms,inputs); /* program */
                                   /* output terms */

       if ((row+1) != terms)   /* because of odd number */
                               /* of CCELLSP */
          {

           /* program CCELLR & CCELLSP */

           x1 = x2 = 7 + inputs*LCCELL + 10 +
                col*LCCELLR;
           y1 = 13 + (terms-1)*WCCELLR +
                (terms-1)*WCCELLSP -
                row*WCCELLR - row*WCCELLSP;
           y2 = 13 + (terms-1)*WCCELLR +
                (terms-2)*WCCELLSP -
                row*WCCELLR - row*WCCELLSP;
           clfwrite(fpo,CCELLR,x1,y1,0,0,0);
           clfwrite(fpo,CCELLSP,x2,y2,0,0,0);
          ]


       else
          {
           x1 = 7 + inputs*LCCELL + 10 +
                col*LCCELLR;
           y1 = 13;
           clfwrite(fpo,CCELLR,x1,y1,0,0,0);
          }


      if (row == 0)            /* program CGNDCON */
       {
         y = 13 + terms*WCCELLR +
             (terms-1)*WCCELLSP + 3;
         x = 7 + inputs*LCCELL + 10 +
             17 + col*LCCELLR;              /* rotate */
         clfwrite(fpo,CGNDCON,x,y,0,-1,0);  /* 90 degrees */


         if(col == 0)      /* program right Gnd buss */
           {
```

```
                    y1 = y2 = 13 + terms*WCCELLR +
                              (terms-1)*WCCELLSP +
                              LCGNDCON + 2;
                    x1 = x + 1;
                    x2 = x1 + (outputs -1)*LCCELLR + 2;
                    fprintf(fpo,"L NM;\n");
                    fprintf(fpo,"W 4 %d,%d %d,%d;\n",x1,y1,x2,y2);
                  }
              }

            if ((row+1) == terms)
              {

                y = 0;                          /* programPlaOut*/
                x = 7 + inputs*LCCELL + 10 +
                    17 + col*LCCELLR +1;
                cifwrite(fpo,PlaOut,x,y,0,0,0);

                /* program output clock options */
                progopt(fpo,inputs,col,clkin,clkout,clkboth,'o');

                if(col == 0)     /* program VDD buss wire */
                  {
                    y1 = y2 = 2;
                    x1 = 7 + inputs*LCCELL + 18;
                    x2 = x1 + outputs*LCCELLR - 8.5;
                    fprintf(fpo,"L NM;\n");
                    fprintf(fpo,"W 4 %d,%d %d,%d;\n",x1,y1,x2,y2);
                  }

                /* program Pla output pieces */

                x1 = 7 + inputs*LCCELL + 10 +
                     3 + col*LCCELLR + 7;
                x2 = x1 - 7;
                y1 = 13;
                y2 = 13;
                cifwrite(fpo,CCONNE3,x1,y1,0,-1,0);
                cifwrite(fpo,CCONNE2,x2,y2,0,-1,0);
              }
          }
      }
  }

/*************************************************************
*                                                            *
*  The following implements module 1.4 (Terminate CIF File)  *
*                                                            *
*************************************************************/

  /* calculate Pla size */

  if(clkin == 0 && clkout == 0 && clkboth == 0)
```

```
        {
          lysize = 4 + terms*WCCELL + 9;
        }
      else if(clkin == 1 || clkboth == 1)
        {
          lysize = terms*WCCELL + 9 + WPlaClkin;
        }
      else
        {
          lysize = 4 + terms*WCCELL + 9 + WPlaClkOut;
        }

      ixsize = 7 + inputs*LCCELL + 11 + outputs*LCCELLR;
      fprintf(fpo,"DF;\n");     /* CIF terminating command */
      fprintf(stderr,"(external pla (cif %d bounds 0,0 %d,%d));\n",
            symbnm,ixsize,lysize);

  exit(0);
}
```

```
/*****************************************************************
*                                                                *
*       NAME:  errcheck (Error Check)                            *
*       MODULE NUMBER:  1.1                                      *
*       FUNCTION:  checks input and output terms for improper    *
*                  characters                                    *
*       INPUTS:  string, pcheck, opt                             *
*       OUTPUTS:  none                                           *
*       CALLING MODULES:  main                                   *
*       MODULES CALLED:  none                                    *
*                                                                *
*****************************************************************/

errcheck(string, pcheck, opt)
   char string[200];
   char *pcheck, opt;
      {
         if(opt == 'I')
            {
               if(*pcheck != '0' && *pcheck != '1' && *pcheck != '-')
                  {
                     fprintf(stderr,
                           "Bad input term (%c) in line: %s\n",
                            *pcheck,string);
                     exit(1);
                  }
            }
         else
            {
               if(*pcheck != '0' && *pcheck != '-')
                  {
                     fprintf(stderr,
                           "Bad output term (%c) in line: %s\n",
                            *pcheck,string);
                     exit(1);
                  }
            }
         return;
      }
```

```
/*****************************************************************
*                                                                *
*       NAME:  clfwrite  (Write to CIF File)                     *
*       MODULE NUMBER:  1.3.1.1.1                                *
*       FUNCTION:  writes CIF statements and coordinates to      *
*                  output file                                   *
*       INPUTS:  fpo, symbnm, x, y, rx, ry, m                    *
*       OUTPUTS:  none                                           *
*       CALLING MODULES:  main, proginp, progout                 *
*       MODULES CALLED:  none                                    *
*                                                                *
*****************************************************************/

int clfwrite(fpo,symbnm,x,y,rx,ry,m)
    int symbnm,x,y,rx,ry,m;
    FILE *fpo;
    {
      if ((rx == 0 && ry == 0) && m == 0)
          fprintf(fpo,"C %d T %d %d;\n",symbnm,x,y);
      if ((rx == 0 && ry == 0) && m != 0)
          fprintf(fpo,"C %d M X T %d %d;\n",symbnm,x,y);
      if ((rx != 0 || ry != 0) && m == 0)
          fprintf(fpo,"C %d R %d %d T %d %d;\n",symbnm,rx,ry,x,y);
      if ((rx != 0 || ry != 0) && m != 0)
          fprintf(fpo,"C %d M X R %d %d T %d %d;\n",symbnm,rx,ry,x,y);
     return;
    }



/*****************************************************************
*                                                                *
*       NAME:  proginp (Program Input Terms)                     *
*       MODULE NUMBER:  1.3.2                                    *
*       FUNCTION:  generates CIF coordinates for NMOS, PMOS,     *
*                  and HOLESP Pla pieces required to program     *
*                  input terms                                   *
*       INPUTS:  fpo, pcheck, row, col, terms                    *
*       OUTPUTS:  none                                           *
*       CALLING MODULES:  main                                   *
*       MODULES CALLED:  clfwrite                                *
*                                                                *
*****************************************************************/

proginp(fpo,pcheck,row,col,terms)
      char *pcheck;
      int row, col, terms;
      FILE *fpo;
      {
         int clfwrite();
         int x1, y1, x2, y2, x3, y3;

         /* program ones */
```

```
if(*pcheck == '1')
  {
     x1 = 7 + col*LCCELL;
     y1 = y3 = terms*WCCELL - row*WCCELL - 3;
     x2 = x1 + 14.5;
     y2 = (terms-1)*WCCELL - row*WCCELL + 4.5;
     x3 = x1 + LNMOS;
     clfwrite(fpo,NMOS,x1,y1,0,0,0);
     clfwrite(fpo,PMOS,x2,y2,0,0,1);
     clfwrite(fpo,HOLESP1,x3,y3,0,0,0);
  }

 /* program zeroes */
 if(*pcheck == '0')
  {
     x1 = 7 + col*LCCELL + 10;
     y1 = y3 = terms*WCCELL - row*WCCELL - 3;
     x2 = x1 + 0.5;
     y2 = (terms-1)*WCCELL - row*WCCELL + 4.5;
     x3 = x1 - LHOLESP2;
     clfwrite(fpo,NMOS,x1,y1,0,0,0);
     clfwrite(fpo,PMOS,x2,y2,0,0,0);
     clfwrite(fpo,HOLESP2,x3,y3,0,0,0);
  }

  /* program dashes (no transistors) */
  if(*pcheck == '-')
   {
      x1 = 7 + col*LCCELL;
      y1 = y2 = terms*WCCELL -row*WCCELL -3;
      x2 = x1 + LNMOS;
      clfwrite(fpo,NSPACE,x1,y1,0,0,0);
      clfwrite(fpo,HOLESP1,x2,y1,0,0,0);
   }

return;
}
```

```
/*****************************************************************
*                                                                *
*       NAME:  progout (Program Output Terms)                    *
*       MODULE NUMBER: 1.3.2                                     *
*       FUNCTION:  generates CIF coordinates for NMOS, PMOS,     *
*                  and NSPACE PLA pieces necessary to program    *
*                  output terms                                  *
*       INPUTS:  fpo, pcheck, row, col, terms, inputs            *
*       OUTPUTS:  none                                           *
*       CALLING MODULES:  main                                   *
*       MODULES CALLED:  cifwrite                                *
*                                                                *
*****************************************************************/

progout(fpo,pcheck,row,col,terms,inputs)
     char *pcheck;
     int row, col, terms, inputs;
     FILE *fpo;
      {
         int cifwrite();
         int x1, y1, x2, y2;

            if((row+1) != terms)    /* program all but last row */
               {

                  /* program ones */
                  if(*pcheck == '-')   /*program NMOS & PMOS */
                    {
                       x1 = 7 + inputs*LCCELL + 10 +
                            col*LCCELLR + 17;
                       y1 = 13 + (terms)*WCCELLR +
                            (terms-1)*WCCELLSP -
                            row*WCCELLR - row*WCCELLSP;
                       x2 = x1 - 14;
                       y2 = y1 + 0.5;
                       cifwrite(fpo,NMOS,x1,y1,0,-1,0);
                       cifwrite(fpo,PMOS,x2,y2,0,-1,0);
                    }

                  /* program zeroes (no transistors) */
                  if(*pcheck == '0')      /* program NSPACE */
                    {
                       x1 = 7 + inputs*LCCELL + 10 +
                            col*LCCELLR + 17;
                       y1 = 13 + (terms)*WCCELLR +
                            (terms-1)*WCCELLSP -
                            row*WCCELLR - row*WCCELLSP;
                       cifwrite(fpo,NSPACE,x1,y1,0,-1,0);
                    }


               if((row+1) == terms)        /* program last row */
                  {
```

```
                /* program ones */
                if(*pcheck == '-')
                   {
                       x1 = 7 + Inputs*LCCELL + 10 +
                            col*LCCELLR +17;
                       y1 = y2 = 27;
                       x2 = x1 - 14;
                       clfwrite(fpo,NMOS,x1,y1,0,-1,0);
                       clfwrite(fpo,PMOS,x2,y2,0,-1,0);
                    }

                /* program zeroes (no transistors) */
                if(*pcheck == '0')
                   {
                       x1 = 7 + Inputs*LCCELL + 10 +
                            col*LCCELLR + 17;
                       y1 = 27;
                       clfwrite(fpo,NSPACE,x1,y1,0,-1,0);
                    }

            }

        return;
    }
```

```
/*****************************************************************
*                                                                *
*       NAME:  progopt (Program Clocking Options)                *
*       MODULE NUMBER:  1.3.3                                    *
*       FUNCTION:  determines which clocking options have        *
*                  been chosen and calculates CIF coordinates    *
*                  needed to place the required cells            *
*       INPUTS:  fpo, inputs, col, clkin, clkout, clkboth, c     *
*       OUTPUTS:  none                                           *
*       CALLING MODULES:  main                                   *
*       MODULES CALLED:  clfwrite                                *
*                                                                *
*****************************************************************/

progopt(fpo,inputs,col,clkin,clkout,clkboth,c)
    int inputs, col, clkin, clkout, clkboth;
    char c;
    FILE *fpo;
    {
        int x,y;

        if(clkboth)
            {
               clkin = clkout = 1;
            }

        if(c == 'i' && clkin)
            {
               x = 9 + col*LPlaClkin;
               y = 4 - WPlaClkin;
               clfwrite(fpo,PlaClkin,x,y,0,0,0);
            }

        else if(c == 'o' && clkout)
            {
               x = 7 + inputs*LCCELL + 11 +
                   col*LPlaClkOut;
               y = 0 - WPlaClkOut;
               clfwrite(fpo,PlaClkOut,x,y,0,0,0);
            }

        return;
     }
```

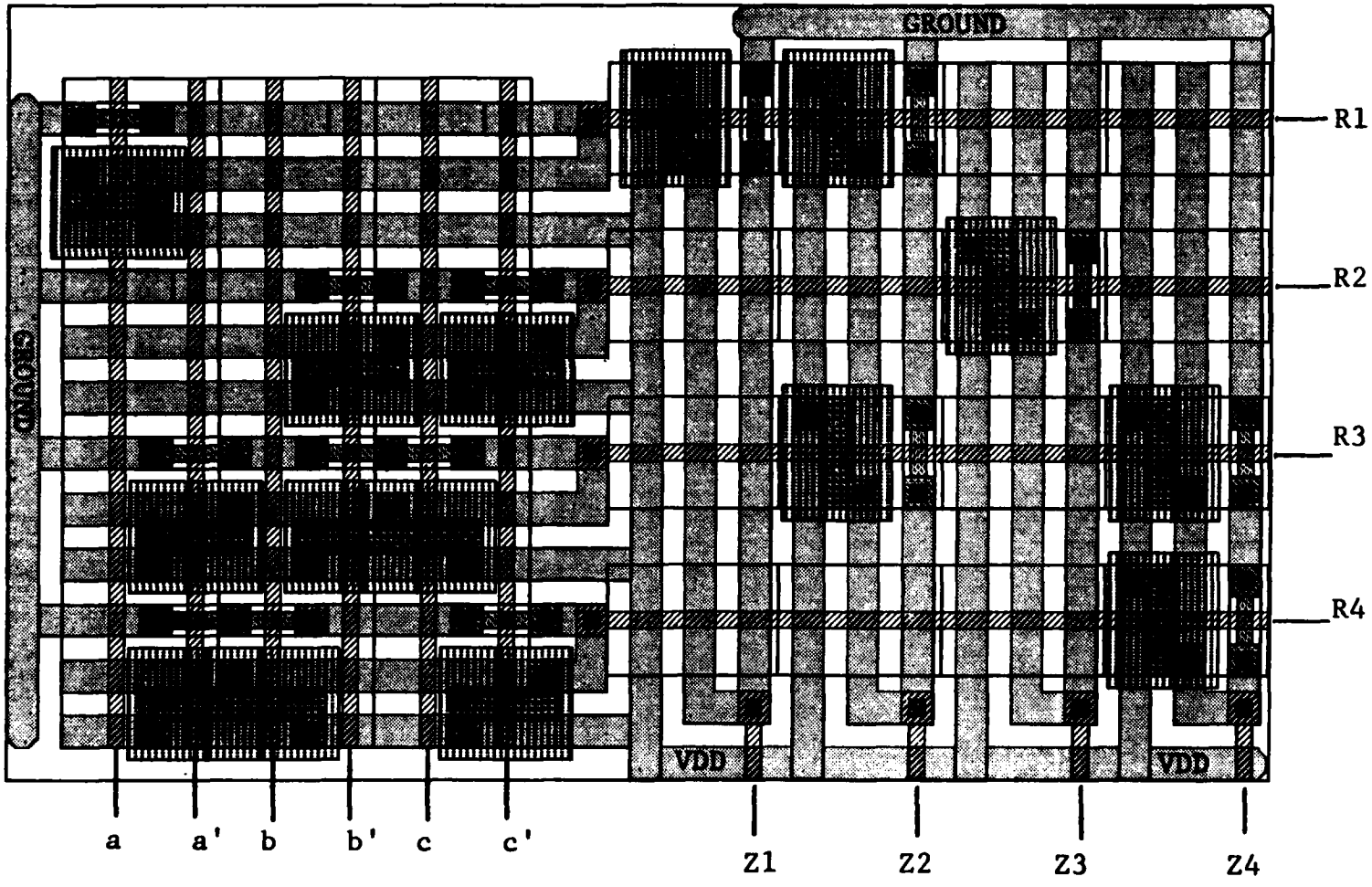


Figure E-1 Basic PLA Without Clocking

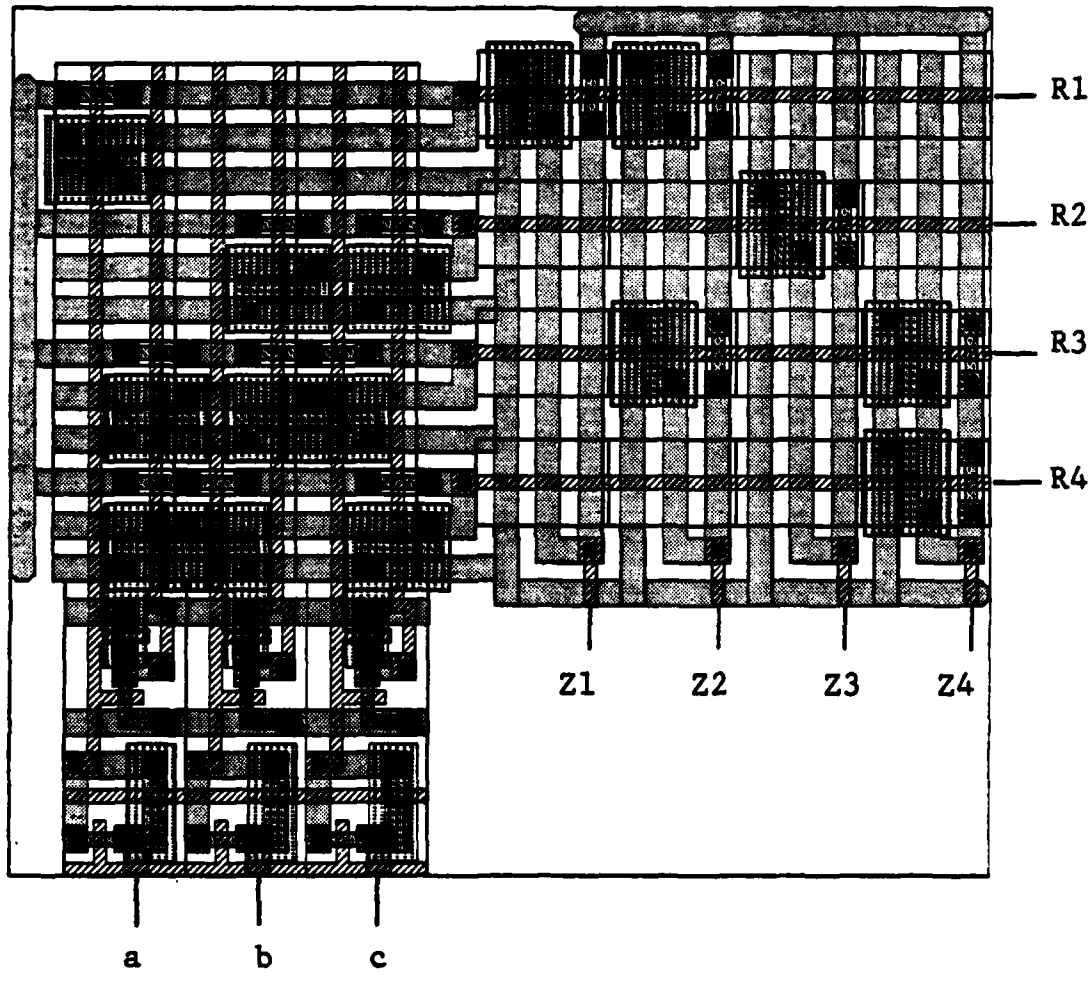


Figure E-2 PLA With Clocked Inputs

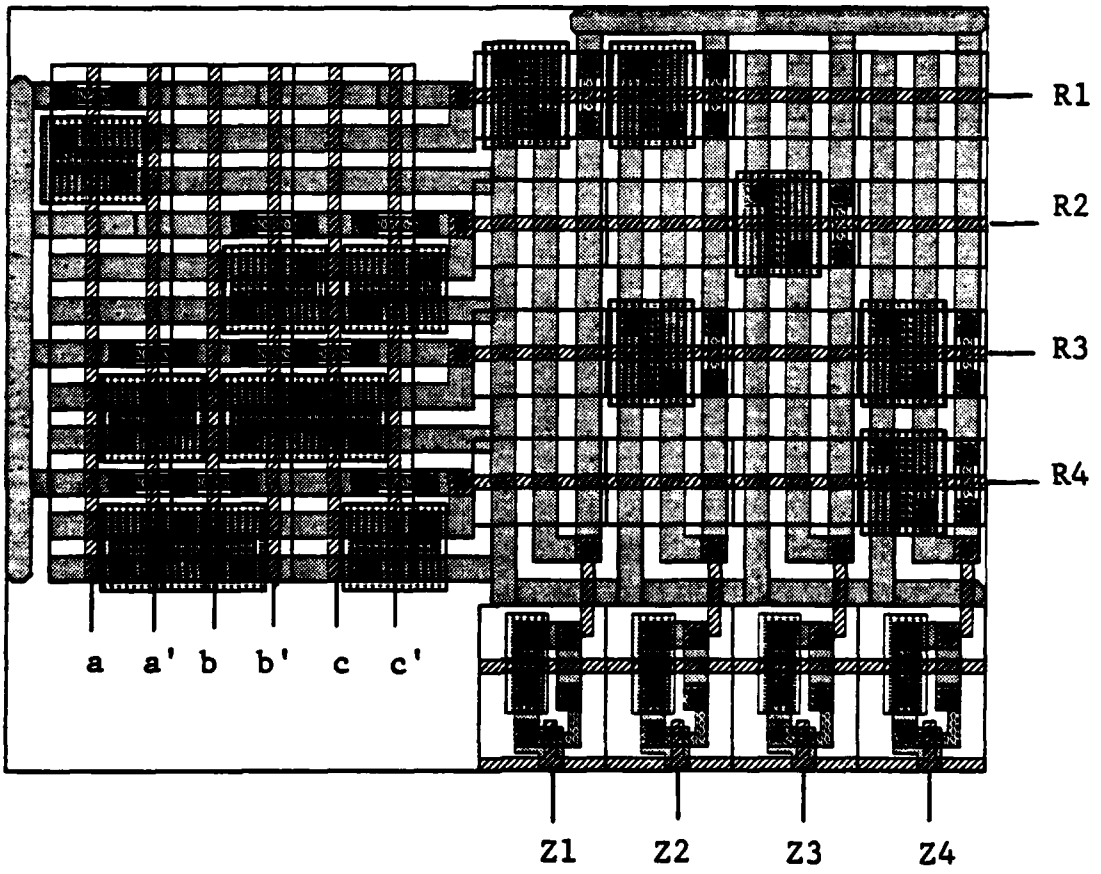


Figure E-3 PLA With Clocked Outputs

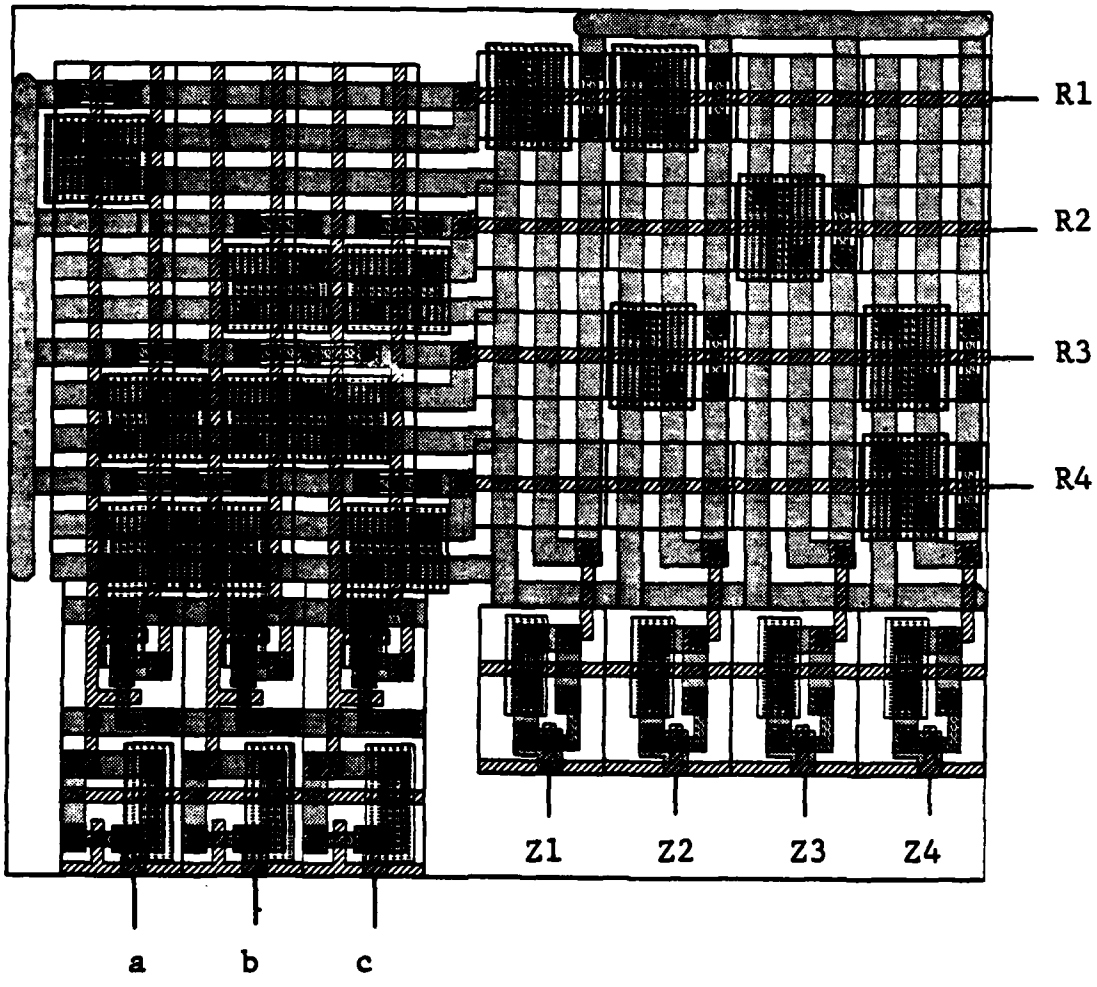


Figure E-4 PLA With Clocked Inputs and Clocked Outputs

Appendix F. 4-Bit ALU Implementation

A discussion of the layout of the ALU is presented. Testing deficiences that were encountered are also discussed, and several CLL plots of the final layout are provided. Additionally, a procedure for converting CIF formatted files from NMOS specifications to CMOS/SOS specifications is presented.

Layout

Physical layout of the ALU corresponds very closely to the logic gate representation shown in Chapter V (see Figure V-7). The only difference is the location of the transmission gates which clock-in operand selects S0-S3. They were moved to the lower left section of the circuit to help reduce the size of the layout.

Essentially, there are two distinct types of interconnections or busses; vertical and horizontal. With the exception of the two-phase clock paths and carry-in and select lines, all long vertical busses are either Vdd or ground wires. These wires are all 4 lambda wide and overlay Vdd and ground wires contained in the standard cells. This method was deemed more time efficient than interconnecting all Vdd and ground lines separately. The metal-to-metal overlap should not effect performance. In order to simplify completion of the layout, all Vdd paths are connected to a larger wire 6 lambda wide that traverses the bottom of the

chip. The Vdd pad connection may be made at any point along this buss. Additionally, all ground paths are connected to a larger 6 lambda wire but at the top of the chip. Similarly, the ground pad connection may be made at any point along the buss.

All other horizontal paths represent data paths. All data signals enter the left side of the chip and exit the right side. PHI1 and PHI2 enter the top of the chip. Inputs include operands A0 through A3 and B0 through B3, CARRY-IN, SELECT, function selects S0 through S3, and complemented and uncomplemented PHI1 and PHI2 clock signals. Outputs include result F0 through F3, CARRY-OUT, and P and G. The latter two outputs may be used with a high-speed external look-ahead carry circuit.

The CLL plot of Figure F-1 shows the general locations of all inputs and outputs. Exact locations are labled on the enlarged plots of Figures F-2 through F-5. These enlarged plots represent areas or windows of the chip that are enlarged to show more detail. Each window represents 25% of the chip. Beginning at the upper left corner of the chip and then moving clockwise, Figures F-2 through F-5 respectively, show these quarter sections.

Obviously, no pads were available to complete the layout. Nevertheless, the layout is completed to such an extent that pads and associated connecting wires can be easily added when they become available. A total of 27 pads are required.

Testing

Due to the large size and complexity of the layout, only very limited modular-type testing was accomplished. The SPICE analysis of individual standard cells provided a low-level verification of cell performance. Additional design rule testing using the NMOS design rule checker was performed. Implant surround errors were the only errors that resulted, and these were simply the sum of all errors for the individual standard cells. The main concern regarding possible errors though, is with the hundreds of interconnecting wires between individual cells. The size of the ALU makes SPICE analysis prohibitively complex and increases the chance of oversight during manual inspections. Without a switch-level simulator, there is no method to positively verify the operational integrity of the ALU.

A possible solution that should be examined is that of finishing the layout with crude test pads and then submitting the layout for fabrication. But because of the cost involved with fabrication (CMOS/SOS is much more expensive than NMOS fabrication because of difficulties in making the sapphire substrate), this alternative must be studied carefully.

NMOS to CMOS/SOS Conversion

Once the decision has been made to submit a design for fabrication, the NMOS layers and NMOS lambda must be changed to CMOS/SOS layers and CMOS/SOS lambda throughout

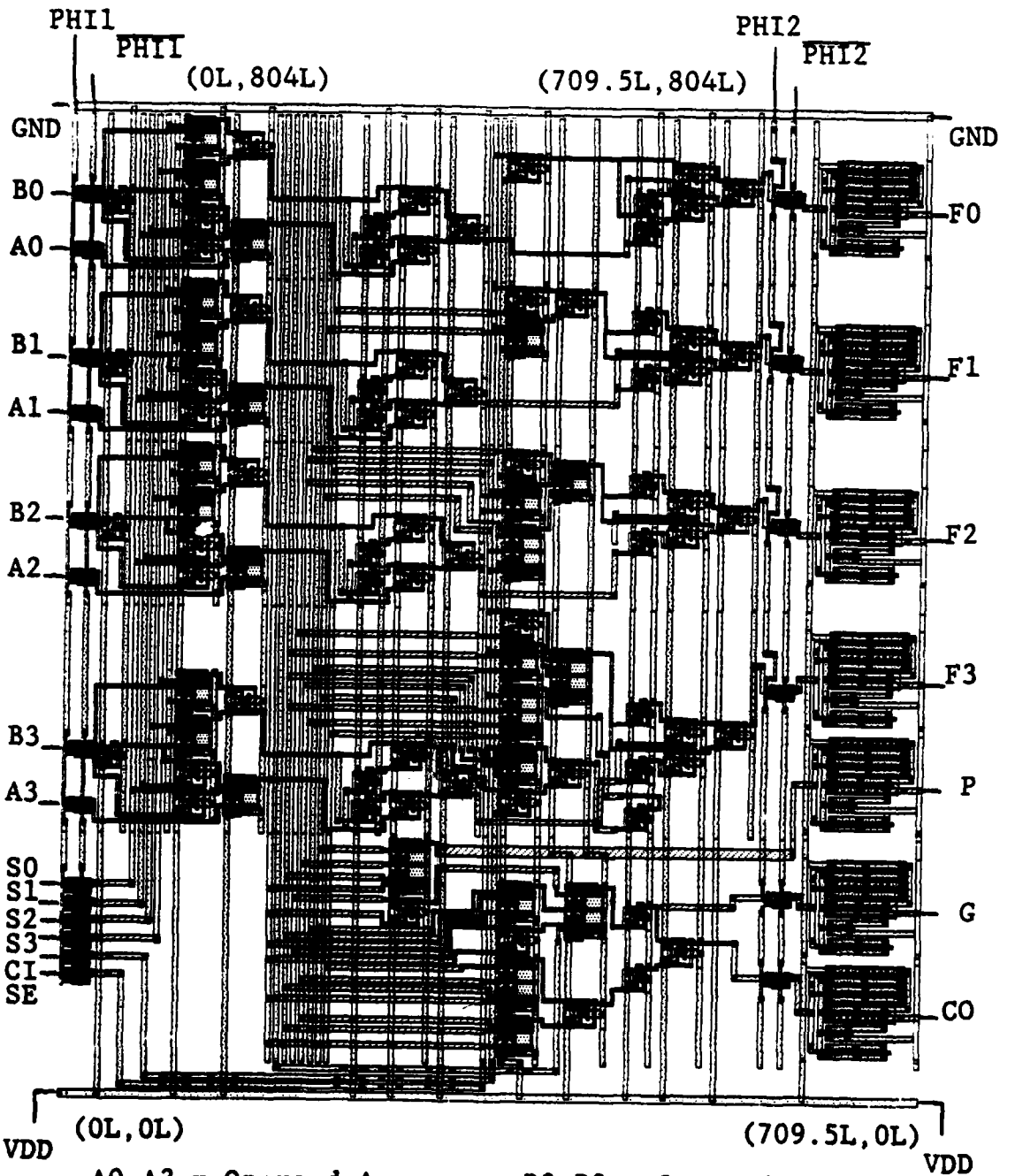
the CIF formatted file. Table A-1 summarizes both the NMOS and CMOS/SOS layers that were discussed in Chapter II.

Layer conversion is a simple process in which the NMOS layers within the CIF formatted file are changed to the corresponding CMOS/SOS layers. This may be done globally with appropriate editing commands.

Table F-1 NMOS and CMOS/SOS CIF Layers

NMOS Layer	CMOS/SOS Layer
ND - Diffusion	SIS - Island
NI - Implant	SIM - PMOS Implant
NP - Polysilicon	SP - Polysilicon
NC - Contact Cut	SC - Contact Cut
NM - Metal	SM - Metal
NB - Buried Contact	Not Allowed
NG - Overglassing	SG - Overglassing

Converting to the CMOS/SOS lambda is also easily accomplished. Lambda appears several places within each symbol definition in a CIF formatted file. For NMOS, lambda appears as lambda divided by two with units of microns (2.5/2 x 100 = 125). The 125 should be replaced with the corresponding CMOS/SOS lambda which is 4/2 x 100 = 200. To simplify global replacement, lambda is always separated from the scaling factor "1" by a "/" (i.e. 125/1). Table F-2 is a partial listing of a CIF formatted file that will fabricate the two input NAND gate. This table shows the fabrication-ready file "final.cif" that results from the "cll -F" command. Table F-3 shows the file with all references to NMOS layers and NMOS lambda replaced with CMOS/SOS layers and CMOS/SOS lambda.



A0-A3 = Operand A
B0-B3 = Operand B
F0-F1 = Result F
S0-S3 = Function Select
CI = Carry In
CO = Carry Out
PHI1 = Phase 1 of clock
PH2 = Phase 2 of Clock

SE = Arithmetic or Logic Select

P and G are used with external carry circuit

Figure F-1 Complete 4-Bit ALU CLL Plot

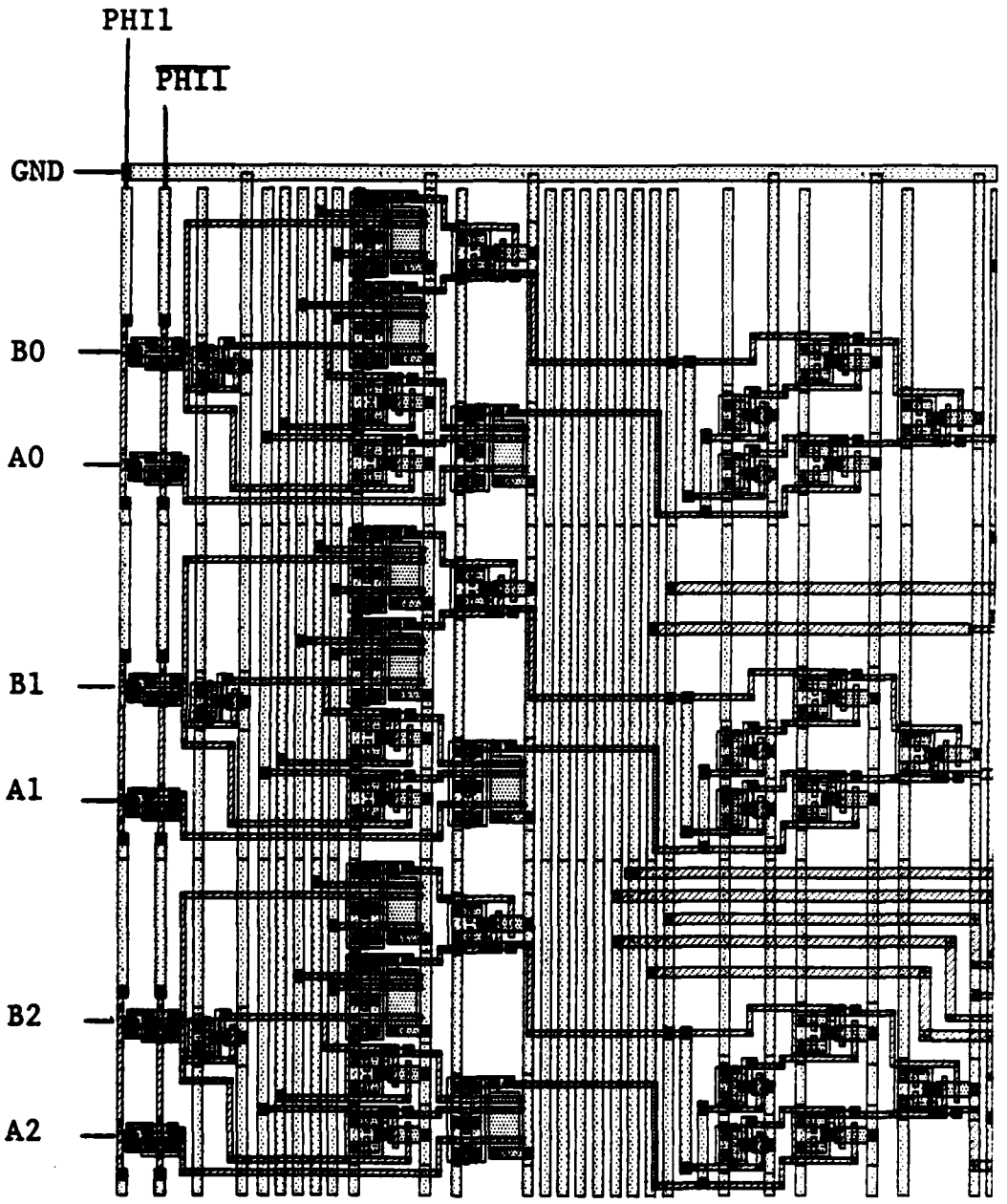


Figure F-2 Upper Left Section of 4-Bit ALU

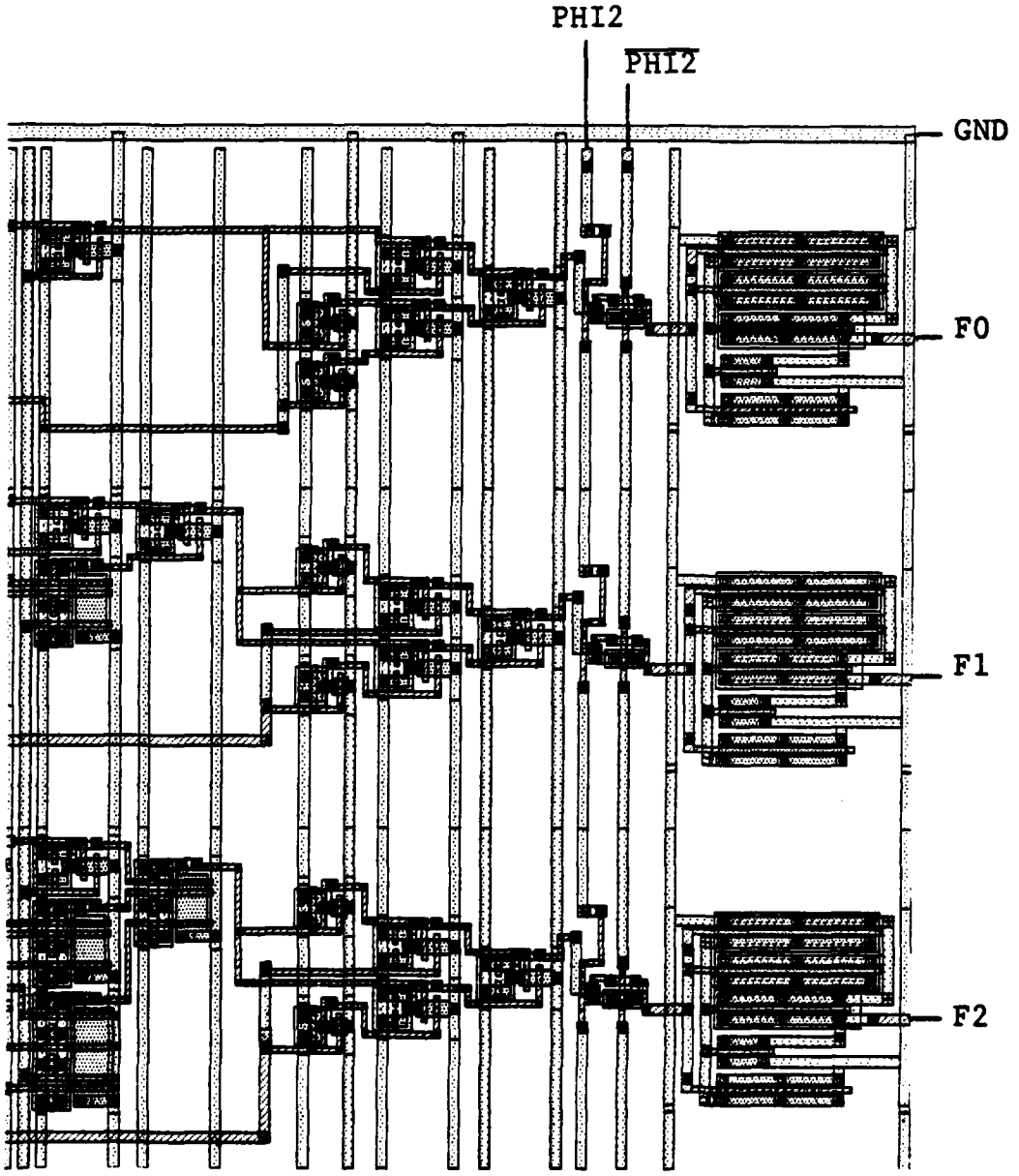


Figure F-3 Upper Right Section of 4-Bit ALU

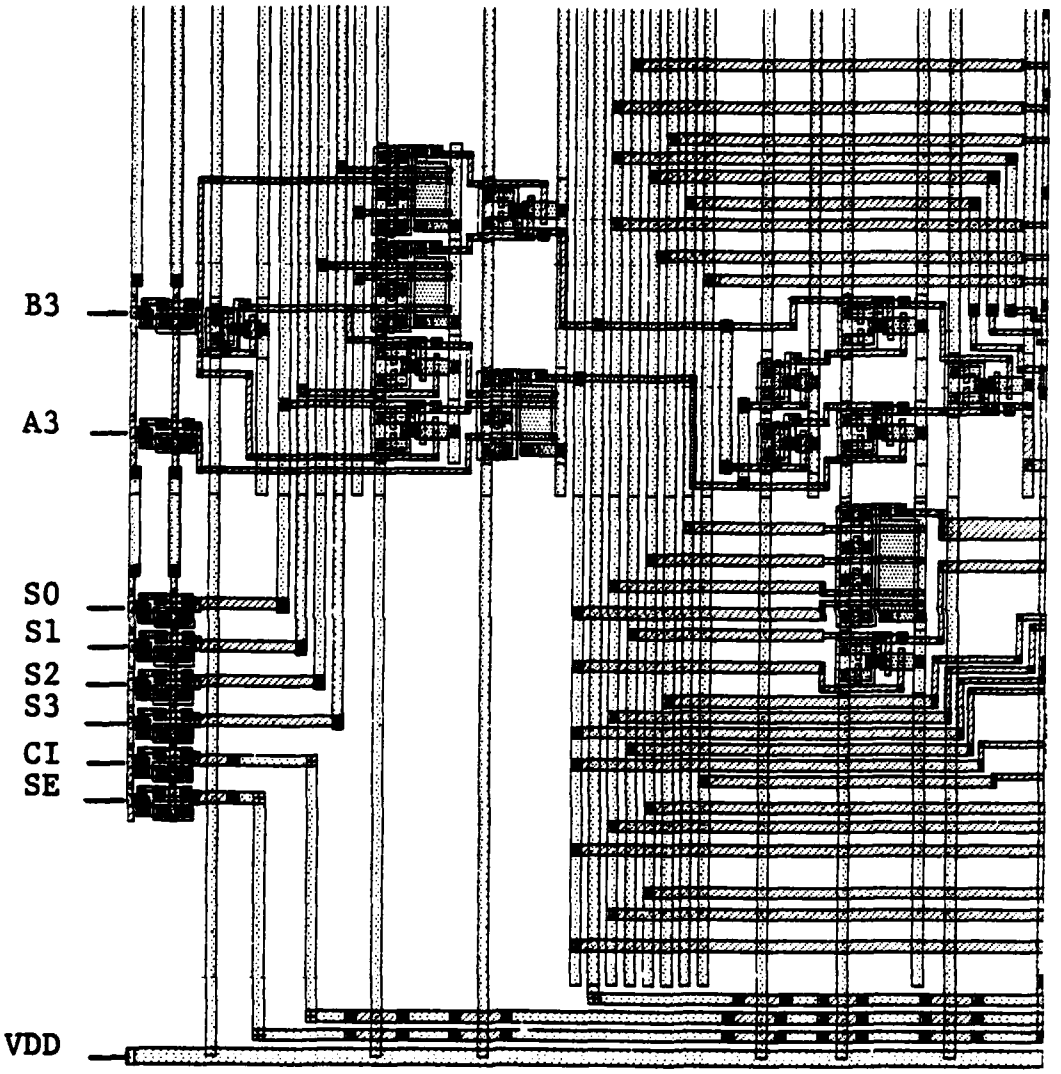


Figure F-4 Lower Left Section of 4-Bit ALU

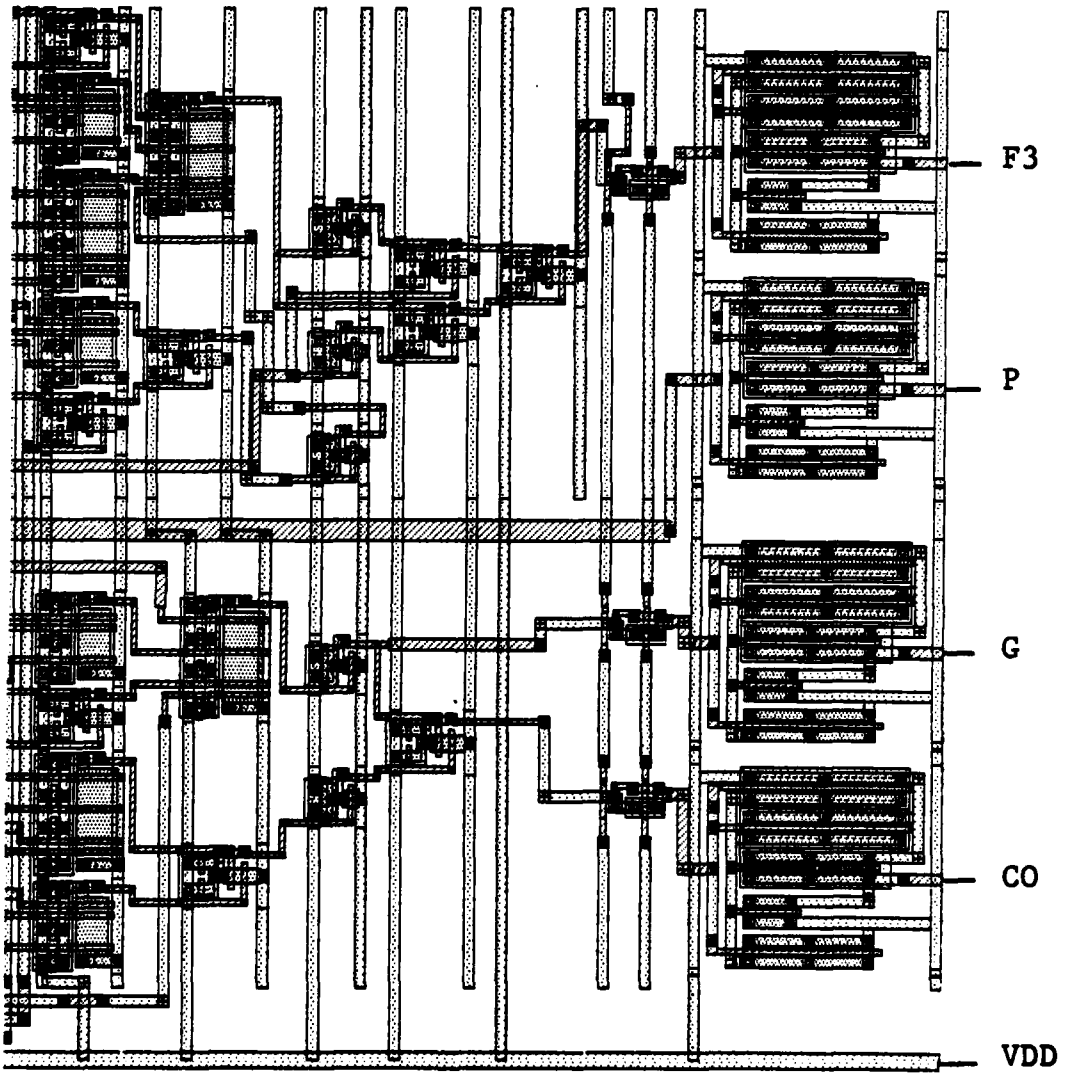


Figure F-5 Lower Right Section of 4-Bit ALU

Table F-2 NMOS CIF Formatted File

```
(ent 953);
(ent 1001);
DS 953 125/1;
(TITLE NAND2 953);
L ND;
B 24 8 12,14;
B 24 8 12,34;
B 4 12 22,24;
      "
      "
      "
L NC;
B 8 4 27,24;
L NI;
B 30 34 12,24;
L ND;
B 8 8 4,14;
L NM;
B 8 8 4,14;
L NC;
B 4 4 4,14;
L ND;
B 8 8 4,34;
L NM;
B 8 8 4,34;
L NC;
B 4 4 4,34;
L ND;
B 8 8 61,24;
L NM;
B 8 8 61,24;
L NC;
B 4 4 61,24;
L NP;
B 8 8 47,42;
L NM;
B 8 8 47,42;
L NC;
B 4 4 47,42;
(bounds NAND2: -1.5,0.0 34.0,24.0);
DF;
DS 1001 125/1;
(TITLE nand 1001);
C 953 T 3 0;
(bounds nand: 0.0,0.0 34.0,24.0);
DF;
C 1001 T 0,0;
E
```

Table F-3 CMOS/SOS CIF File

```
(ent 953);
(ent 1001);
DS 953 200/1;
(TITLE NAND2 953);
L SIS;
B 24 8 12,14;
B 24 8 12,34;
B 4 12 22,24;
     "
     "
     "
B 6 6 28,41;
L SC;
B 8 4 27,24;
L SIM;
B 30 34 12,24;
L SIS;
B 8 8 4,14;
L SM;
B 8 8 4,14;
L SC;
B 4 4 4,14;
L SIS;
B 8 8 4,34;
L SM;
B 8 8 4,34;
L SC;
B 4 4 4,34;
L SIS;
B 8 8 61,24;
L SM;
B 8 8 61,24;
L SC;
B 4 4 61,24;
L SP;
B 8 8 47,42;
L SM;
B 8 8 47,42;
L SC;
B 4 4 47,42;
(bounds NAND2: -1.5,0.0 34.0,24.0);
DF;
DS 1001 200/1;
(TITLE nand 1001);
C 953 T 3 0;
(bounds nand: 0.0,0.0 34.0,24.0);
DF;
C 1001 T 0,0;
E
```

VITA

Wayne Edward Sommars was born on 22 July 1957 in Alton, Illinois. He graduated from Alton Senior High School in 1975 and attended Southern Illinois University at Edwardsville where he received the degree of Bachelor of Science in Electrical Engineering in August 1979. Upon graduation, he was commissioned a second lieutenant in the USAF through the ROTC program. From October 1979 through April 1980 he attended the Basic Communications Electronics Officers' Course at Keesler AFB, Mississippi. He was then stationed at Langley AFB Virginia until May 1982 where he served as a communications electronics engineer. In June 1982, he entered the School of Engineering, Air Force Institute of Technology to pursue a graduate degree in digital engineering and semiconductor device technology. He is a member of Eta Kappa Nu and Tau Beta Pi.

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1. REPORT NUMBER AFIT/GE/83D-62	2. GOVT ACCESSION NO. AD-A138 314	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* THE DESIGN AND LAYOUT OF A COMPLEMENTARY METAL OXIDE SEMICONDUCTOR-SILICON ON SAPPHIRE CELL LIBRARY		5. TYPE OF REPORT & PERIOD COVERED MS Thesis 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Wayne E. Sommars Captain USAF		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Air Force Institute of Technology (AFIT-EN) Wright-Patterson AFB, Ohio 45433		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE December, 1983 13. NUMBER OF PAGES 265
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

Approved for public release: IAW AFR 190-17.

LYNN E. WOLAVER
Dean for Research and Professional Development
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7 Feb 84

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

CMOS
CMOS/SOS
Standard Cell Library
Programmable Logic Array

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A method was developed for designing CMOS/SOS circuits using computer-aided design tools available from Stanford University and The University of California at Berkeley. CMOS/SOS fabrication methods and theory of operation as well as differences between CMOS/SOS and bulk CMOS were researched. Basic logic gates were designed as part of a small CMOS/SOS standard cell library, and a medium scale integration (MSI) arithmetic logic

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19. (continued)
Complementary Metal Oxide Semiconductor
Complementary Metal Oxide Semiconductor-Silicon on Sapphire
SPICE Analysis

20. (continued)

unit (ALU) was developed using cells from the library. SPICE was used to determine optimum gate width-to-length ratios resulting in symmetrical transitional delays. Two designs were developed to implement the CMOS/SOS programmable logic array (PLA), and a "C" program was written to automatically generate one of the designs by means of a file formatted in Caltech Intermediate Form (CIF).


FILM
4-8